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(54) Nozzle structures for bubblejet print devices.

(57) A bubblejet print device (100) is disclosed which is integrally formed having arrays (102,103,104,105) of nozzles (110) which form part of a passageway communicating between opposite surfaces of a semiconductor substrate (130). Each nozzle (110) has an integrally formed heater (120) which permits heating of ink (106) within the respective nozzle (110) for the ejection of an ink drop (108) therefrom. The heater (120) can provide a fault tolerant structure through the provision of a main heater (121,441) and a redundant heater (122,443) each of which can be separately energised from a corresponding electronic drive circuit (160,165). Several methods of manufacturing the device (100) using semiconductor fabrication techniques are also disclosed. A bubblejet print head (200) incorporating the device (100) can form part of an image reproducing apparatus (531,533,535,537) and is capable of printing full colour images at 400 dpi and monochrome images up to 1600 dpi. An ink drop size of about 3 picolitres is used for these image intensities. A thermal shunt (140) or diffuser (491) are used to transport heat away from the heater (120) to prevent formation of hot spots therabout after the ejection of an ink drop (108). Electronic circuitry (310,302-305) is disclosed which is used to couple data to the device (100) to provide full width page printing using a stationary head (200) and a moving paper medium (220).

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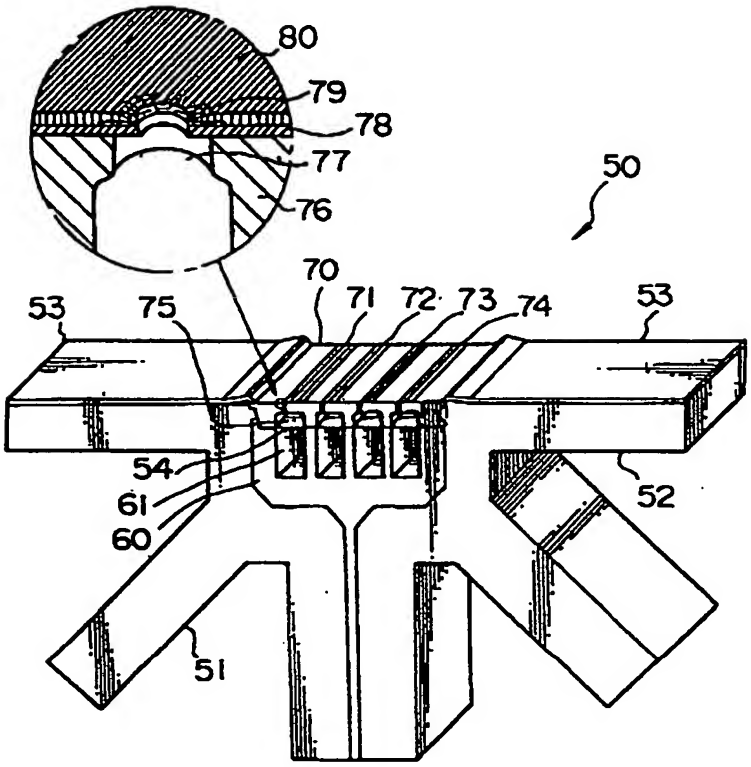
FIG. 4



The present invention relates to ink jet printing and in particular, discloses a semiconductor bubble jet print head.

Bubble jet print heads are known in the art and have recently become available commercially as portable, relatively low-cost printers generally used with personal computers. Examples of such devices are those made by HEWLETT-PACKARD as well as the CANON BJ10 printer.

Figs. 1 and 2 show schematic perspective views of prior art bubblejet print heads representative of those used by CANON and HEWLETT-PACKARD, respectively.

As seen in Fig. 1 the prior art bubblejet (BJ) head 1 is formed by a BJ semiconductor chip device 2 abutting a laser etched cap 3. In this configuration, the cap 3 acts as a guide for the inward flow of ink (indicated in the drawing by arrows), into the head 1 via an inlet 4, and the outward ejection of the ink from the head 1 via a plurality of nozzles 5. The nozzles 5 are formed as the open ends of channels in the cap 3. Upon the BJ chip 2 are arranged one or more (generally 64) heater elements (not shown) which are energised so as to cause ink to be ejected from each of the nozzles 5 by a bubble of vapourised ink formed within the corresponding channel. The BJ chip 2 also includes a semiconductor diode matrix (not illustrated) which acts to supply energy to the heater elements arranged adjacent the channels.

In the prior art HEWLETT-PACKARD thermal ink jet head 10 as seen in Fig. 2, a two part configuration is also used, however ink enters the cap 12 through an inlet 13 arranged in the side of the cap 12 which supplies an array of nozzles 14 arranged perpendicular to the inlet 13. Ink exits through the face of the cap 12. A flat heater 15 is arranged immediately beneath each nozzle 14 so as to cause ejection of ink from the inlet channel 13 into the nozzles.

However, problems exist with these prior art devices due to their two-part construction in creating accurate registration between the two parts. Even if accurate registration were initially achieved, differing rates of thermal expansion or contraction would prevent this accuracy being maintained over appreciable dimensions. Such registration problems limit performance of the prior art devices to image densities generally lower than 400 dots per inch (dpi), and scanning or moving print heads rather than fixed print heads.

It is an object of the present invention to substantially overcome, or ameliorate, the above mentioned problems through provision of an alternative bubble jet print head configuration.

The present invention relates to bubblejet print technology and deals with one or more of the following aspects:

- a bubblejet print devise that is integrally formed; that is, a bubblejet print device comprising a plurality of nozzles each communicating with a corresponding passageway for the supply of ink to the nozzle, and heater means associated with each the passageway or nozzle, characterised in that the nozzles, passageways and heater means are integrally formed.
- an assembly of such bubblejet print devices;
- an image reproducing apparatus using such a bubblejet print device;
- a bubblejet print head including such a bubblejet print device;
- a bubblejet print device having nozzles supplied with ink or different colours;
- a data phaser for the bubblejet print device;
- a bubblejet print device in which the heater arrangement for each nozzle or passageway surrounds the nozzle or passageway;
- a bubblejet print device in which each nozzle and passageway extends between a pair of opposite faces of the device;
- a bubblejet print head including a bubblejet print device of length substantially equal to the width of the paper (i.e. dimension of the paper to be printed transverse the direction of relative motion past the device);
- such a bubblejet print head in which electrical power connections to the device are made substantially along the entire length of the device;
- a bubblejet print device having nozzles arranged in rows, the nozzles of each row being offset in the row direction relative to the nozzles of the adjacent row or rows;
- a method of fabricating the bubblejet print device;
- an integrated electronic structure having an integrated thermal conductor to transport heat from one part of the structure to another part of the structure;
- a bubblejet print device in which each heater arrangement for each nozzle has a plurality of heaters each having a corresponding electronic drive circuit;
- a bubblejet print device in which each heater arrangement has a plurality of electronic drive circuits in which the heaters and the corresponding electronic drive circuits are spaced apart in relation to each other;

- a bubblej t print d vice having at l ast on set of redundant nozzles and a main set of nozzles with the h at rs of the corresponding redundant nozzles being operabl on d t ction of a failur of th heaters of the corr sponding main nozzl ; and
- a bubbl j t printing ass mbly having a plurality of bubbl jet printing d vic s in which for each intended print location a sensing circuit is provided to interconnect corresponding heaters of the devices to sense the failure of one of the corresponding nozzle heater and subsequently operate one other of the corresponding nozzles.

As used herein, the term "a Z-Axis bubblejet chip (ZBJ chip)" is used to describe a chip lying in the x y plane in which ink flows both into and out of the chip in the z direction.

The above and other objects, effects, features and advantages of the present invention will become more apparent from the following description of embodiments thereof taken in conjunction with the accompanying drawings.

A number of preferred embodiments of the present invention will now be described with reference to the drawings in which:

Figs. 1 and 2 are representations of prior art BJ print heads;
Fig. 3 is a representation of a ZBJ chip of the present invention;
Fig. 4 is a cut-away isometric view of a first embodiment of a ZBJ print head;
Fig. 5 is a view similar to Fig. 4 but of a second embodiment;
Figs. 6 to 9 illustrate one etching process which can be used to create the ZBJ nozzles;
Figs. 10, 11 and 12 illustrate one possible arrangement of the heater elements within the ZBJ substrate;
Fig. 13 shows an alternative heater configuration;
Figs. 14 to 23 show various alternate nozzle configurations;
Figs. 24 to 31 show the manner of expulsion of ink from one nozzle of the ZBJ chip;
Figs. 32 to 36 illustrate the transfer of heat about the ZBJ chip;
Fig. 37 and 38 show the configuration of a ZBJ print head including a chip, membrane filter and ink channel extrusion;
Figs. 39 and 40 illustrate ink drop positions for a single pixel using a four nozzle per pixel print head and a single nozzle per pixel print head respectively;
Fig. 41 is a timing chart illustrating nozzle firing order;
Fig. 42 shows nozzle firing patterns for a one nozzle per pixel colour print head;
Fig. 43 shows nozzle firing patterns for a four nozzles per pixel colour print head;
Fig. 44 is an exploded perspective view of a thin section of the full colour ZBJ print head assembly of Fig. 5;
Figs. 45 and 46 illustrate the deflection angle imparted on the ink drop due to the main and redundant heaters respectively;
Figs. 47 and 48 show two methods of connecting power to the ZBJ chip;
Fig. 49 shows an arrangement of heaters in a prior art BJ head;
Fig. 50 shows the arrangement of heater drivers within the preferred embodiments;
Fig. 51 shows a heater driver including a transfer element;
Fig. 52 is a timing diagram of pulses used for driving the heaters;
Fig. 53 shows the circuit arrangement of a heater driver using a single clock pulse;
Fig. 54 shows the circuit arrangement of a clock regeneration scheme;
Fig. 55 shows a circuit arrangement for regenerating pulse widths within the clock line;
Fig. 56 is a schematic black diagram of the data driving circuit configuration used for the ZBJ head;
Fig. 57 is a block diagram representation of the data phaser ASIC of Fig. 56;
Figs. 58A and 58B show two alternate configurations of the main and redundant heaters;
Fig. 59 shows one circuit stage of a ZBJ driver implementing digital fault tolerance;
Fig. 60 is a schematic circuit diagram of a similar circuit using analog fault tolerance;
Fig. 61 is a one circuit stage of ZBJ driver using complete redundancy;
Fig. 62 illustrates both the electrical and physical layout of the drivers of the ZBJ chip;
Fig. 63 shows a power wiring loop necessary for the arrangement of Fig. 58;
Fig. 64 illustrates one circuit stage of a ZBJ circuit designed for large area fault tolerance;
Figs. 65, 66 and 67 show other fault tolerant configurations;
Figs. 68, 69 and 70 illustrate preferred configurations for th manufactur of multipl ZBJ heads on a singl silicon waf r;
Figs. 71 to 80 illustrate th various stages used in wafer processing of th ZBJ chip;
Fig. 81 is a cross-sectional sch matic view through a wid hol which incorporates sev ral nozzles;
Figs. 82 to 113 show th manufacturing stages of a pr ferred embodim nt;

Fig. 114 is a schematic block diagram representation of a colour photo copier incorporating a colour ZBJ head;

Fig. 115 is a similar representation of a colour facsimile machine;

Fig. 116 is a similar representation of a printer for a computer;

Fig. 117 is a similar representation of a video printer; and

Fig. 118 is a similar representation of a simple printer.

Table 1 lists details of ZBJ chips for various applications; and

Table 2 lists various fault conditions and their consequence.

Referring firstly to Fig. 3, the general configuration of a Z-axis bubblejet (ZBJ) chip 40 is shown which includes an ink inlet arranged on one (underside as illustrated) plane surface of the chip 40 and a plurality of nozzles 11 which provide for outlets of ink on the opposite side. It is readily apparent from a direct comparison of Figs. 1 and 2 with Fig. .3 that in the ZBJ chip 40, is provided as a single, monolithic, integrally formed structure as opposed to the two part structure of the prior art. The chip 40 is formed using semiconductor fabrication techniques. Furthermore, ink is ejected from the nozzles 41 in the same direction that ink is supplied to the chip 40.

Referring now to Fig. 4, a cross-section of a first embodiment of a stationary (i.e. non-moving) ZBJ printhead 50 is shown which is configured for the production of full length A4 continuous tone colour images at an image density of 1600 dpi or 400 pixels per inch. The head 50 is provided with a ZBJ chip 70 having four nozzle arrays, one for each of cyan 71, magenta 72, yellow 73 and black 74. The nozzle arrays 71-74 are formed from nozzle vias 77 with four nozzles per pixel giving a total of 51,200 nozzles per chip 70. The magnified portion, of Fig. 4 shows the basic nozzle cross-section which is formed in a silicon substrate 76 over which a layer 78 of thermal SiO_2 is formed. A heater element 79 is provided about the nozzle 77 which is capped by an overcoat layer 80 of chemical vapour deposited (CVD) glass. Each of the nozzles 77 communicates to a common ink supply channel 75 for that particular colour of ink. The ZBJ chip 70 is positionable upon a channel extrusion 60 which has ink channels 61 communicating with the channels 75 so as to provide for a continuous flow of ink to the chip 70. A membrane filter 54 is provided between the extrusion 60 and the chip 70.

Two power bus bars 51 and 52 are provided which electrically connect to the chip 70. The bus bars 51 and 52 also act as heat sinks for the dissipation of heat from the chip 70.

Fig. 5 shows a second embodiment of a ZBJ head 200 similar in configuration to that shown in Fig. 4.

The head 200 has a ZBJ chip 100 including nozzle arrays 102, 103, 104 and 105 for each of cyan, magenta, yellow and black respectively. The chip 100 has ink channels 101 which communicate with ink reservoirs 211, 212, 213 and 214, respectively for the above colours, in a channel extrusion 210.

The channel extrusion 210 has an alternate geometry of higher volumetric capacity than that shown in Fig. 4 for the same size of the chip 100. Also illustrated are tab connections 203 and 204 which connect the power bus bars 201 and 202 to the chip 100. A membrane filter 205 is also provided as before.

So as to be able to print an A4 page, the head 200 is required to be about 220 mm long, by 15 mm across, by 9 mm deep. Using the foregoing as a standard arrangement, many configurations of ZBJ heads are possible. The actual size and the number of nozzles per chip depends solely on the required performance of the printer application.

Table 1 lists seven applications of ZBJ printheads and the various requirements for each application considered necessary. Application one is considered suitable for low cost full colour printers, portable computers, low cost colour copiers and electronic still photography. Application two is considered suitable for personal printers, and personal computers, whilst application three is useful in electronic still photography, video printers and workstation printers. The fourth application finds use in colour copiers, full colour printers, colour desktop publishing and colour facsimile. The fifth application is for a monochrome devise which sees application in digital black and white copiers, high resolution printers, portable computer's, and plain paper facsimiles. Applications six and seven show respectively high speed and medium speed A3 continuous tone applications useful in colour copiers and colour desktop publishing. The high speed version of application six finds use in small run commercial printing and the medium speed version in colour facsimile.

It will be appreciated by those skilled in the art that the foregoing applications are configured for ZBJ heads with a drop size of 3 pl (pico-litres). Other configurations are possible and that higher operating speeds can be achieved at the expense of image quality, by using larger drop sizes.

The physical structure of the ZBJ chip 100 will now be described in detail. The ZBJ chip 100, as illustrated in Fig. 5, for example, has four nozzle arrays 102-105, each comprising four rows of nozzle vias 110 (Figs. 6-9). The nozzle vias 110 are formed by etching through a substrate 130 of the chip 100. The substrate 130 is generally about 500 microns deep and depending on the required application, can be 220

mm long by 4 mm wide. Figs. 6 to 9 illustrate th etching of the nozzl vias 110 through the substrat 130. So that the ZBJ chip 100 can j ct a drop of 3 pl, it is necessary for the diam ter of each nozzl 110 to be approximat ly 20 micr ns. In one possibl manufacturing m thod a four stag proc ss is used comm ncing with a 500 micron deep substrat 300 having an overlying glass (SiO_2) layer 142 nclosing a h at r 120 within as seen in Fig. 5. Firstly, the step as seen in Fig. 6 is a plasma etch of a 20 micron straight-walled round hole, through the glass overcoat 142 and at least 10 microns into the substrate 130. This forms the nozzle tip 111.

The next step as seen in Fig. 7 requires the etching of a large channel (approximately 100 microns wide by 300 microns deep) in the rear of the chip 100. This forms nozzle channels 114 that supply ink flow to the nozzles 110. The neat step, as seen in Fig. 8, is to print nozzle barrel patterns at the bottom of the channels 114 formed in Fig. 7. The nozzle barrels 113 are approximately 40 microns in diameter and are plasma etched to within 10 microns of the front of the chip 100. As the an isotropic plasma etch is relatively non-selective, this method cannot be used to etch the entire cavity without also etching through, and destroying the heater 120.

Accordingly, as seen in Fig. 9, an isotropic etch is used on all exposed silicon to a depth of 10 microns from the front of the chip 100. This step acts to widen the nozzles 110 and undercut the SiO2 layer 142 containing the heater 120. This step forms the nozzle cavity 112. The step also ensures that the tip 111 join the barrel 113 without risking plasma etched damage to the heater 120. It will be apparent to those skilled in the art that the above mentioned dimensions are only approximate and show a general concept only. However, the front to back surface etching should be aligned to better than 10 microns and the etch depth control should also be better than 10 microns. In this way, the complete nozzle via 110 is formed including its tip 111, cavity 112, barrel 113 and channel 114.

It will be apparent that, the formation of the nozzle tip 11, nozzle cavity 112 which acts as a thermal chamber, nozzle barrel 113 and nozzle channel 114 creates a passageway for the flow of ink through the substrate 100 for ejection.

Prior art integrated bubblejet heads manufactured by Canon use hafnium boride (HfB_2) as the heater element 120. The present Canon BJ10 printer has heater parameters selected for a drop size of 65 pl. The drop size of 3 pi as used in the preferred embodiments of the present invention, being substantially smaller, retires re-dimensioning of the heater configuration. So as to ensure that high temperatures are reached, whilst maintaining heater resistance and minimising overall size, a serpentine design as seen in Fig. 10 can be used. Furthermore, as seen in Fig. 10, the heater 120 comprises two heating elements which take the form of a main heater 121 and a redundant heater 122 arranged about, and surrounding the nozzle tip 111. The redundant heater 122 is provided so as to increase the fault tolerance of the ZBJ chip 100 thereby increasing the yield of the manufacturing process. This configuration of the heaters 120 contrasts with the prior art where, because of the two part structure, the heaters reside on the BJ chip which forms only one of the channel walls.

Fig. 11 shows a cut-away section of the nozzle via 110 of Figs. 6 to 10. In particular, the relative dimensions of the heater 120 and nozzle tip 11 can be assessed.

Fig. 12 represents a cross-section along the lines A-A'-B- B' of Fig. 10 of a single, complete, nozzle thermal chamber. The substrate 130 is generally a silicon wafer approximately 200 microns thick (thinned from a 500 micron wafer by back-etching after high temperature processing). The substrate 130, in addition to providing ink paths and thermal paths for waste heat, also acts as a semiconductor substrate for driver electronics which connect to the heater 120.

A thermal insulation layer 132 is provided as a 0.5 micron layer of thermally grown SiO2. The layer 132 has several functions including providing electrical insulation for the heater 120 from an overlying passivation layer 144, providing mechanical cushioning of the heater 120 from the force of a collapsing vapour bubble, and acting as an integral part of a MOS driver circuit (to be later described). To allow for the best heat transfer from the heater 120 to the ink 106, the thermal layer 132 is preferably manufactured to be as thin as possible without sacrificing reliability. As the layer 132 is thermally grown SiO_2 and not CVD SiO_2, it has no pin holes. Thus, it is possible for it to be thinner than the corresponding layer on prior art bubblejet heads.

The heater 120 is a 0.05 micron layer of hafnium boride or other compound of group IIIA to VIA metal borides. This provides a high electrical resistance element to convert an electrical driving pulse to a thermal puls . Th very high m lting point of HfB_2(3100°C) m ans that th r is a substantial margin in th actual h at r temperatur . The electrical contact to the heater 120 is provided by a heater contact 123 comprised of 0.5 microns of aluminium. This is formed part of a first metal level 134.

Th first m tal l vel 134 is a lay r of aluminium 0.5 microns thick. Th first l v l 134 is formed at th sam tim as the contacts 123 to the heaters 120. This layer provides conn ctions b tw n th h aters 120

and th driv l ctronics (to be d scribed), as w ll as connections within th driv l ctronics. It is to b noted that for th colour ZBJ heads described in this specification, ther ar a larg number or nozzles 110 in a small ar a, requiring a high interconnection d nsity and fine lin width. B cause of this, int rconnection siz s of the ord r of 2 microns ar required.

An interlevel insulation layer 136 is provided as a layer of CVD SiO_2 or PECVD SiO_2 (PE = photon enhanced), approximately 1 micron thick. The thickness of the layer 136 is important to the operation of the ZBJ chip 100, as it provides a thermal lag between the heater 120 and a thermal shunt 140, thereby ensuring that the majority of the heat is transferred to the ink 106 rather than to the substrate 130. The interlevel insulator 136 also provides the electrical insulation between the first metal level 134 and a second metal level 138, but in thin role, the thickness is not critical.

A second metal level 138 is provided and forms the second level of electrical interconnections as well as the thermal shunt 140. The interconnection density of the high speed ZBJ heads earlier described (with 250 nozzles per linear millimeter) is high enough to require two levels of metal if 2 micron design rules are used. Other head designs may only require one level of metal. If one level of metal is used, an alternative arrangement for the thermal shunt 140 is required, as this is formed on top of the interlevel oxide 136.

The thermal shunt 140 is formed from a disc of aluminium approximately 0.5 microns thick. The shunt 140 is thermally connected to the substrate 130 through vias 410 in the thermal layer 132 and the interlevel layer 136, but serves no electrical purpose. The purpose of the thermal shunt 140 is to couple waste heat from the heater 120, to the substrate 130 at a controlled rate. The heat must be substantially removed in the period between heater energisation pulses, so that the quiescent temperature of the ink 106 remains low.

It is intended that the thermal shunt 140 be formed at the same time as the second metal level 138. This is possible if the thickness of the thermal shunt 140 corresponds to that of the second metal level 138. The required thickness is determined by the quality of heat coupling between the thermal shunt 140 and the heater 120. The actual amount of heat coupling required is best determined by accurate computer modelling for the particular nozzle geometry used. The amount of heat coupling can be varied from that illustrated (in Figs. 32-35 to be described hereafter) either by etching holes in the heat coupling disc of the shunt 140 so as to decrease the thermal conductivity. Alternatively, the thermal coupling can be increased by increasing the thickness of the shunt 140 and/or replacing it with a material of higher thermal conductivity, such as silver.

Another purpose of the thermal shunt 140 is to prevent a overcoat 142 formed of thick CVD glass from being heated. This will slow CVD carrier gas diffusion through the thick layer 142, and therefore slow the formation of gas bubbles which can destroy the heater 120.

The overcoat 142 is a thick layer of CVD or PECVD glass, and has three functions. Firstly, to provide the nozzle for ink ejection, secondly to provide mechanical strength to resist the shock of exploding or collapsing vapour bubbles, and thirdly to provide protection against the external environment.

Because the ZBJ chip 110 must be exposed to air for the printing process to operate, its surface therefore requires increased levels of protection than that required for hermetically sealed devices. The thickness of the overcoat 142 can be about 4 microns although this can be substantially thicker to provide adequate nozzle length.

A passivation layer 144 is provided by means of a 0.5 micron layer of tantalum, or other materials, which is conformably coated over the entire structure of the chip 100 to provide chemical and mechanical protection thereto.

Finally, the ink 106 in Fig. 12, as well as having the obvious function of providing the printing mechanism, also acts to remove waste heat. A 3 pl drop of ink generally removes 13 nJ of heat for each degree celsius that its temperature has been raised.

In Fig. 13, an alternate configuration of the heater is shown. Here, a heater 440 has a main heater 441 and a redundant heater 443 each of which are annular and surround the nozzle 445 out of which an ink drop 446 is ejected.

The heaters 441 and 443 are made of deposited HfB2 and are interlaced by overlapping aluminium connections 442 and 443 (respectively). With this configuration, the heater 440 surrounds the underlying thermal cavity 447 and can therefore produce an annular ink vapour bubble (see Figs. 24 to 31). This bubble therefore tends to exert near equal pressure to all sides of the ink drop 446. Because the main heater 441 and redundant heater 443 are identical with respect to shape and location, they have identical drop jection charact ristics. Th heat rs 441 and 443 ar also slightly ecc ntric with r sp ct to th nozzle 445 and so th drop jection angl does not chang significantly if the main heater 441 fails and the redundant h ater 443 is used.

Although Fig. 12 illustrates a nozzl 110 having a cylindrical cavity 112 and narrow r tip 11, forming an underlying thermal chamber or cavity 115, various alternative nozzle geometri s ar also useful, som of

which are illustrated in Figs. 14 to 23.

In Fig. 14, the thermal chamber 115, which surrounds the nozzle tip 111 is arranged as a cylinder, with the heater 120 deposited in the walls of the cylinder. This arrangement has several disadvantages, including:

-(1) the heater film must be deposited vertically inside the cylinder and whilst this can he achieved by chemical vapour deposition (CVD), it is then very difficult to etch the heater 120 into the required size and shape;

-(2) it is difficult to achieve a redundant heater configuration for fault tolerance (to be later described);

-(3) the heater 120 must be buried below the surface so that there is ink 106 to eject, or the vapour will simply vent out of the tip 111; and

-(4) the ink is separated from the heater 120 by CVD SiO2 instead of crystalline SiO_2, which has a higher thermal conductivity.

In Fig. 15, the thermal chamber 115 is arranged as a cone. This is to allow the heater 120 to be etched to increase its resistance. This arrangement has the following difficulties:

-(1) if the cone angle is made too shallow, the nozzle 110 will not fill with ink 106 by capillary action.

-(2) if the cone angle is made too steep, like the cylindrical chamber it is still difficult to etch the heater 120; and

-(3) the nozzle barrel 123 is very narrow, thus increasing the ink refill time.

Fig 16 shows a quasi-hemispherical chamber in which the heater 120 is formed on a frusto-conical section which faces into a substantially hemispherical chamber.

Figs. 17 to 22 show six preferred nozzle structures which permit monolithic construction, a small drop size of 3 picolitres thus permitting 1600 dpi printing, fault tolerant heater design, nozzle spacing anywhere on the surface of the substrate and permitting use in multi-colour print devices. Further, more detailed discussion of the fabrication of the following nozzle structures can be found later in this document.

Fig. 17 illustrates a substantially hemispherical thermal chamber 115 and which is formed by applying an undercutting isotropic plasma etch of silicon before reactive ion etching (RIE) of the nozzle barrel 113. This configuration is characterised by a reverse action in which the formation of the bubble 116 is in the direction opposite to the ejection of the ink drop 108. The thermal shunt 140 conducts heat away from the nozzle area into the substrate 130 to reduce the time taken for the thermal chamber 115 to cool sufficiently prior to the ejection of the next ink drop 108.

This configuration has advantages of planar construction of the heater 120 whereby accurate control of the heater shape and size can be achieved. Also, the thermal coupling between the heater 120 and the ink 106 is significant, because the heater 120 is isolated from the ink 106 by the thermal SiO2 layer 132 which is more thermally conductive than CVD glass. Also, this layer can be manufactured thinner than a corresponding layer of CVD glass, as it is not prone to pinholes. Depending on the slope of the barrel 113 as it enters the thermal 115, and the contact angle of the ink with the passivation layer 144 (see Fig. 12), this nozzle geometry will permit automatic filling by capillary action.

Disadvantages of this configuration reside in the reversed operation by which bubble formation is in the opposite direction to ink ejection which reduces efficiency. Also, the thick CVD glass overcoat 142 is required which forms the nozzle region. Finally, waste heat must be dissipated via a long path through approximately 600 microns of silicon substrate 130. This limits the nozzle density and/or the maximum firing rate of the nozzles. Other disadvantages relate to potential difficulties with the nozzle 111 filling with ink 106, by capillary action, if the angle of the barrel 113 and and the thermal chamber 115 are not closely monitored.

Fig. 18 is similar to the configuration of Fig. 17 except that in this geometry, the direction of flow of ink 106 through the chip 100 is reversed giving a reversed nozzle arrangement 485 in which bubble formation is in the same direction as ink drop ejection.

As seen in Fig. 18, ink 106 enters the nozzle passageway through an aperture 481 and a meniscus 107 is formed at the nozzle tip 486 boundary between the barrel 487 and the channel 489. Formation of bubbles 116 acts to expel an ink drop 108 through the channel 489 and onto a medium such as paper 220.

The configuration of the reverse nozzle arrangement 485 differs in one significant way from the earlier configurations described. The earlier configurations (e.g. Fig. 17) utilise a thermal shunt 140 which acts to shunt heat away from the heater 120 and into the substrate 130. However, in the configuration of Fig. 18, immediately adjacent the heaters 120 is an underlying reservoir of ink 106. Accordingly, a thermal diffuser 491 is used to increase the area of heat transport from the heater 120 through the overcoat 142 and into the ink 106 reservoir. In this configuration, because the heat conductive path is much shorter than that of Fig. 17, greater heat dissipation can be achieved. Also, heat dissipation can be further enhanced by re-circulating the ink 106 through a heat exchanger using a supply pump (not illustrated).

This configuration has the advantages of planar construction, good th rmal coupling and heat dissipation. Also, bubbl direction is in the direction of ink ejection which reduces kin tic losses. A disadvantage of this configuration is that th nozzl is not self priming, and must b initially primed using positiv pressur . Once primed, th shrinking bubbl will draw ink into the thermal chamb r 488 aft r the drop 108 has been fired. Also, the cantilevered section supporting the heaters 120 must be sufficiently thick to withstand the shock from collapsing bubbles 116.

Turning now to Fig. 19, a nozzle arrangement is shown which includes a trench implanted heater 493. In this embodiment, the nozzle cavity 112 is formed as a straight cylinder communicating with the nozzle barrel 113 and the optionally etched nozzle channel 114. An annular trench 492 is etched into the silicon, and a layer of SiO2 is grown adjacent and about the nozzle cavity 112. The annular heater 493 is plated on the trench 492 which acts to form vapourised bubbles 116 which expand across the cavity 112 transverse the direction of drop ejection. Advantages of this configuration include good thermal coupling and self-priming. Disadvantages includes poor heat dissipation because liquid cooling by forced ink flow is not effective as the bulk of the ink is isolated from the bubble generating surface by 600 microns of substrate 130. Also, it is difficult to obtain adequate nozzle length as this must be generated by very thick layers of CVD glass forming the overcoat 142. Additionally, bubble formation being transverse permits non-optimal motion coupling. Also, thermal conduction into the substrate 130 is high causing heat to be wasted therethrough. Finally, the length of the heater 493 is constrained by the circumference or the nozzle, or half the circumference if fault tolerance is employed, and so it is difficult to obtain a high resistance heater 493.

Fig. 20 illustrates the annular trench configuration of Fig. 19 shown in the reversed arrangement. Here the annular trench 492 extends towards the nozzle tip 486 as does the diffused heater 493 therein. A thermal diffuser 491 is also provided in the previous manner. Unlike Fig. 19, due to the configuration of the channel 489 the nozzle length can be easily varied. Advantages of this configuration reside in thermal coupling, case of heat dissipation, self priming and ease of manufacture. Disadvantages include the bubble direction being transverse to the direction of ink drop ejection, and difficulty in controlling the length of the heater 493. Also, thermal conduction to the silicon substrate 130 is high which causes heat to be wasted.

Fig. 21 shows a further configuration utilising an elbow heater. In this embodiment, a cylindrical nozzle passageway is formed between the nozzle tip 111 and the barrel 113. Thermally grown SiO2 is provided as a layer 494 which extends into the barrel 113. An elbow oriented heater 495 is then plated onto the layer 494 and an electrical contact 496 made on the top surface of the heater 495. Overcoat layer 142 of CVD SiO_2 is then provided over the contact and heater and extends into the nozzle barrel 113. Advantages of this configuration are self priming and thermal insulation of the heater 495 from the substrate 130. Disadvantages include poor heat dissipation, difficulties in controlling the nozzle length by varying the thickness of the overcoat 142, transverse bubble direction, poor thermal coupling due to the heater 495 being isolated from the ink 106 by a layer of amorphous CVD glass, difficulties in controlling heater length, and manufacturing complexity (described later).

Fig. 22 illustrates the reverse arrangement of the elbow connected heater 495 which is manufactured in a similar manner. Advantages include heat dissipation through the ink reservoir, self priming and the heater 495 being thermally insulated from the substrate 130. Disadvantages include transverse bubble direction, poor thermal coupling through the amorphous CVD glass between the heater 495 and ink 106, and constraints to the heater length.

Fig. 23 illustrates a nozzle arrangement similar to that of Fig. 18, however the relative sizes of the nozzle aperture 484 and the nozzle tip 486 have been varied to improve capillary action for the filling of the nozzle and the formation of the meniscus 107. One disadvantage of the configuration of Fig. 18 is that the nozzle aperture 484 and the nozzle tip 486 have equal diameters. The diameter of the nozzle tip 486 varies depending on a number of design criteria such as the desired drop size.

In order to prime the nozzle and provided the meniscus 107 as illustrated, the ink 106 must flow through the aperture 484 but then stop at the tip 486. Generally, if both are the same size, the ink will either form a meniscus at the aperture 484, or drip through the tip 486 depending on the priming pressure. Neither of these conditions are desired. What is specifically desired is that the aperture 484 be of sufficient diameter to allow for priming of the nozzle, and that the tip 486 be of a different, smaller diameter to provide for the formation of the meniscus 107. The nozzle is then primed using a pressure greater than the "bubble pressure" of the aperture 484, but less than the "bubble pressure" of the nozzle 486. The configuration of Fig. 23 which illustrates a suitabl arrang m nt wh r in th diam t r of th apertur 484 is approximat ly 50% larg r than that of th tip 486. This configuration also provides for accurate control of the drop siz whilst maintaining high r filling rates of th nozzle.

Th operation of th ZBJ chip 100 differs from that of prior art bubblejet heads through th use of an alternat drop jection mechanism which is illustrated in Figs. 24 to 31. In Fig. 24, a singl nozzl 110 of

the ZBJ print h ad 100 is shown in its quiescent state where th heater 120 is off. Ink 106 within the nozzl 110 forms a m niscus 107.

In Fig. 25, th heat r 120 is turned on thus h ating the surrounding substrate 130 and thermal lay r 132 which in turn h ats th ink 106 within th nozzle 110. Som of th ink 106 evaporat s to form small bubbl s 116.

As seen in Fig. 26, as the evaporated ink 106 is heated, it expands and coalesces into large bubbles 116.

In Fig. 27, pressure from the expanding gas bubbles 116 forces ink 106 out of the nozzle tip 111 at high speed.

In Fig. 28, the heater 120 is turned off which acts to contrast the bubble 116 and draw ink 106 from the drop 108 that is formed.

In Fig. 29, the drop 108 separates from the ink 106 within the nozzle 110 and the contracting bubble 116 draws an ink meniscus 107 backwards into the nozzle 110.

As seen in Fig. 30, surface tension causes the nozzle 110 to refill with ink 106 from the underlying reservoir and in which the velocity of ink 106 causes overfilling.

Finally in Fig. 31, the ink 106 oscillates, and eventually returns to the quiescent state. The oscillating damping time is one factor which determines the maximum dot repetition rate.

As depicted in Fig. 32, when the heater 120 is turned on, a portion of the heat will flow into the ink 106, and the remainder flows into the material surrounding the nozzle in the manner indicated.

Fig. 33 illustrates the super heating of ink in which a thin layer of superheated ink 109 forms adjacent the passivation layer 144 within the nozzle cavity 112.

Excess heat must be rapidly removed after the heater 120 is turned off. Within 200 microseconds of the heater 120 being energized, there should be no ink 106 remaining at a temperature above 100.C, at which bubbles 116 form due to the ink 106 being substantially composed of water. If this is not achieved, the next ink drop 108 will not fire correctly as there will be an insulating layer of vapour between the heater 120 and the ink 106.

The waste heat is removed by three separate paths. Firstly, heat is removed through the ink which acts to raise its temperature slightly. However, the thermal conductivity of ink is low, so the amount of heat removed by this path is also low.

Because the walls of the nozzle 110 are made of silicon from the substrate 130, and have high thermal conductivity, heat dissipation through the walls is fast. However, not all of the bubble 116 will be in contact with the side walls of the nozzle 110.

Also, waste heat is removed through the heater element 120. Heat dissipation through the heater element 120 is important, as no ink vapour must be in contact with the heater 120 when the next drop is fired. Because the bulk of material around the heater 120 is glass, with low thermal conductivity, the thermal shunt 140 is included, to shunt waste heat to the substrate 130. If the removal of this heat can be achieved within approximately 200 microseconds, then it is not necessary to include the thermal shunt 140. Fig. 34 illustrates the heat flow from the cooling bubble 116 as described above.

Fig. 35 also shows waste heat removal paths 125 in which heat will flow through the substrate 130 as the main thermal conduit away from the heater 120. Some of this heat will flow back into the ink 106 and eventually be ejected with subsequent drops 108. The remainder of the heat will flow through the substrate 130 and into the aluminium heat sink (51,52), seen in Fig. 4.

Fig. 36 illustrates the macroscopic heat dissipation for the ZBJ head 200 with 51,200 nozzles printing four colour. If the heater action does not raise the average temperature of the entire head assembly 200 more than about 10.C to 20.C above that of the incoming ink 106, it is not necessary to provide an external cooling mechanism. In this manner, the ZBJ head 200 can be effectively cooled by a steady flow of ink 106 from ink reservoirs 215, 216, 217 and 218 as illustrated. The quantity of ink flow is in direct proportion to the heat generated, as ink 106 is expelled every time the heaters are turned on.

Generally, about 50 watts of electrical power 126 is supplied to the head 200 which outputs a spray 117 of 12,800 drops per colour per 2.00 µs use. This represents an output 127 of about 1.28 ml of ink drops per second at ambient temperature plus 10-20°C. It should also be noted that the driver circuit on the chip 100 also dissipates some power but this is minor compared to that dissipated by the heaters 120 themselves.

However, if the nozzle efficiency (thermal and the substantially smaller kinetic output compared with electrical input) is l ss than that indicated abov , mor heat will be g n rated than can be expelled with the drops without raising the ink temperatur xcessively. In this cas , other heat sinking methods (such as forced air cooling or liquid cooling using th ink) can also be used.

Whil th av rage temperatur of th ZBJ print head 200 is low, th operating t mperatur of th ZBJ h ater l ments 120 is above 300°C. It is important that th activ l m nts (drive transistors and logic) of

th ZBJ chip 100 do not xperi nc this temperatur xtr m . This can be achieved by locating th drive transistors and logic as far from the heater elements 120 as possible. Th se active elem nts can be located at the edg s of th chip 100, leaving only th heat rs 120 and th aluminium connecting lin s in th high temperatur region.

Ink Channel:

As seen in Figs. 37 and 38, a full colour ZBJ print head 200 has four ink channels, one for each of cyan 211, magenta 212, yellow 213 and black 214. These channels 211-214 are formed as an aluminium extrusion 210 and are filtered and sealed against the back of the ZBJ chip 100.

In some applications, the ink channels 211-214 of Fig. 37 are not sufficient to provide adequate ink flow. In such a situation, the extrusion profile of Fig. 38 can be used so as to increase the volume of flow. As seen in Fig. 37, a 10 micron absolute membrane filter 205 is provided between the ink channel extrusion 210 and the ZBJ chip 100 so as protect against ink contamination. If the membrane filter 205 is compressible, then it can also form as a gasket to prevent ink flow between the four colours. The edges of the head assembly 200 are preferably sealed to prevent gas ingress. For the above configuration, a manufacturing accuracy of approximately ± 50 microns need only be maintained.

Blocked Heads:

Two potential sources of blocked heads and these are dried ink and contamination.

When the print head 200 is not in use, the exposed surface will dry out. If it dries too much, the pressure of a bubble 116 will be insufficient to dislodge any dried ink. This problem can be alleviated by:

1. Automatically capping of the head 200 with an air tight seal when not is use;
2. applying a solvent to the front surface of the ZBJ head 200 during a cleaning cycle;
3. The use of a self-skinning ink; and/or
4. A vacuum cleaning system.

The ZBJ chip 100 is susceptible to blockage by particulate contamination of the ink 106. Any particle of a size between 20 microns and 60 microns will permanently lodge in the nozzle cavity 112, as it cannot be ejected with the ink drop 108. A filter such as the membrane filter 205, is included in the ink path to remove all particles larger than 10 microns. This can be a 10 micron bonded fibreglass absolute filter and preferably has a relatively large area to allow sufficient ink flow. This is seen in Figs. 35 and 44.

The continuous tone ZBJ chip 100 with four nozzles 110 per pixel has a degree of tolerance of blocked nozzles 110. A blocked nozzle 110 will result in a 25% reduction of colour intensity for that pixel rather than a complete absence of colour.

Nozzle to Heater Registration:

The existing prior art bubblejet technologies of Canon and Hewlett-Packard's thermal ink jet systems use a two-piece construction to form the nozzles. The heaters are formed on a silicon chip whereas the nozzles are formed using a cap manufactured of a different material. This technique has proven to be highly successful for the production of scanning thermal ink jet heads with moderate numbers of nozzles. However, to achieve full-width A4 printing (i.e. with a stationary head) with very small drop sizes, this technique becomes more difficult. With nozzle pitches of 64 microns and head lengths of 220 mm, differences in thermal expansion between the substrate and the nozzle cap as small as 0.02% are sufficient to cause malfunction. Even small ambient temperature changes will cause this degree of differential thermal expansion if the cap and substrate are made of differing materials. One solution to this problem is to make the cap out of the same material as the substrate, usually silicon. Even if this is done, differences in temperature between the silicon substrate and the silicon cap (caused by waste heat from the heaters) can be sufficient to cause mis-registration.

The ZBJ chip 100 does not suffer from these problems, as the heaters 120, nozzles 110 and ink paths 101 are all fabricated using a single silicon substrate 130. Nozzle to heater registration is determined by the accuracy of the photolithography with which the ZBJ chip 100 is manufactured. Due to the relatively large f ature siz s of this configuration, th r is littl difficulty in nsuring that th nozzl s ar correctly aligned as th ZBJ chip 100 is a monolithic chip capabl of being manufactured using a 2 micron semiconductor proc ss s.

Continuous Ton Images:

As it is difficult to vary the size of drops from a bubblejet head, continuous tone operation is achieved by varying the number of drops.

In the present case, 16 drops per pixel are used to create an image density of 400 pixels per inch. This gives 16 levels of gray tone per pixel. The tonal subtlety required to produce continuous tone image can be produced by standard digital dot or line screening method or by error diffusion of the least significant 4 bits of an 8 bit colour intensity value. This results in a perceived colour resolution of 256 levels per colour, while maintaining a spacial resolution of 400 pixels per inch. There are two nozzle configuration considered herein: one nozzle per pixel; and four nozzles per pixel. In both cases the drop size is assumed to be approximately 3 pl.

Fig. 39 illustrates the ink drop positions for one pixel of a four nozzle per pixel configuration. In this case, the drops are patterns to fill the pixel in a 4 x 4 array of dimensions 64 mm x 64 mm. Horizontal spacing is provided by the spacing between the nozzle 110, and vertical spacing is provided by paper movement. This arrangement provides sufficient linearity in the relationship between the number of drops and the colour intensity. Four nozzles per pixel also allows a print speed four times faster than that of one nozzle per pixel design, with only slightly larger chip area. The effect of a blocked or defective nozzle is also limited by a reduction in colour by 25%.

Fig. 40 shows a single nozzle type and the ink drop positions for one pixel. In this case, the vertical drop spacing is provided by paper movement. If sixteen drops are deposited in a 64 micron pixel, drops are spaced at 4 microns. The pixel is filled horizontally by the flow of wet ink from overlapping drops.

This arrangement has the disadvantages of severe non-linearity in the relationship between the number of drops and the colour intensity, and a lower print speed. The advantage is a lower cost of manufacture than that of the four nozzle per pixel embodiment.

Nozzle Configuration:

There are several factors which affect the optimum configuration of the nozzles 110. These include:

(1) For a print resolution of 400 dpi, 64 micron square pixels are required;

(2) The number of nozzles per pixel has a different effect on the nozzle configuration;

(3) The nozzle barrel 113 diameter affects the nozzle layout because the barrel 113 is larger than the diameter of the drop 108. In the preferred embodiment 100, the barrel 113 is 60 microns in diameter. To maintain mechanical strength of the chip 100, it is assumed that each nozzle 110 must be at least 80 microns from its nearest neighbour;

(4) The firing duty cycle, which is 1:32, allows a 6.25 microsecond heater pulse every 200 microseconds. This gives time for the ink meniscus 107 to stabilise before the next drop 108 is fired;

(5) To prevent major variations in the supply current energising the heaters 120, all of the 32 available time slots allowed by the 1:32 duty cycle are used by an equal number of nozzles 110. This means that:

$$\text{current} \leq \text{number of nozzles} \times \text{nozzle current}/32;$$

(6) If adjacent nozzles 110 are fired in order, then the heat from one nozzle 110 can interfere with the next, and an area may become too hot. To minimise this problem, widely spaced nozzles 110 are fired in sequence. This is the reason why the firing orders, seen in Figs. 42 and 43 (to be described) appear to be unnecessarily complex; and

(7) The optimum arrangement for a colour head is not simply a monochrome head repeated four times. The extra nozzles of the colour head can be used to achieve better thermal distribution.

Fig. 41 shows the use of a head timing which is divided into 32 different time slots, or "firing orders" each separated by 6.25 microseconds. This produces a repeated cycle of 200 microseconds before the same nozzle as fired again.

Movement of the print medium (e.g. paper 220 in Fig. 18) in the 6.25 microseconds between nozzle firings is equivalent to head placement. The nozzles 110 can readily be skewed to cancel any dot skew caused by paper movement, however this skew will be very small.

Referring now to Fig. 42, this shows a possible nozzle layout for a full colour ZBJ head with one nozzle per pixel and 16 drops per pixel. Horizontal spacing of the nozzles 110 is 1 pixel (64 microns). The nozzles 110 are placed in a zig-zag pattern to maintain spacing of at least 80 microns between nozzle barrels 113, in order to maintain the mechanical strength of the head. Such a head design can be produced with three micron lithography.

To compensate for the physical displacement of th nozzl s 110 from a straight lin , line delays must be introduced into the driving circuit. The number of lines delayed is indicated on the right hand side of Fig. 42. Th firing order 225 is indicated in th c ntr of each nozzl 110 and pap r mov ment by th arrow 222.

Fig. 43 shows a nozzle layout for the full colour ZBJ head 200 with four nozzles 110 per pixel, each firing four times per pixel to give 16 drops per pixel. Horizontal spacing of the nozzles 110 is 16 microns (a quarter of a pixel). The nozzles 110 are arranged in 8 rows in zig-zag pattern to maintain at least 80 microns spacing therebetween. The nozzles 110 of the adjacent rows are also positioned (offset to one another) to compensate for any skew caused by paper movement, indicated by the arrow 222. This head design requires 2 micron lithography for nozzle interconnects and drive circuitry.

It should be noted that although the detailed description of this specification concentrates on the four nozzle per pixel configuration, as this is the most difficult, a one nozzle per pixel configuration can be readily derived.

ZBJ Head Assembly:

The head assembly 200 must deal with several specific requirements:
ink supply; ink filtration; power supply; power dissipation; signal connection; and mechanical support.

The ZBJ head 200 with 51,200 nozzles, each of which can eject a 3 pl ink drop every 200 microseconds, can use a maximum of 1.28 ml of ink per second. This occurs when the head 200 is printing a solid four-colour black. As there are four colours, the maximum flow is 0.23 ml per colour per second. If the ink speed is to be limited to around 20 mm per second, then the ink channels 211-214 must have a cross- sectional area of 16 mm^2 each.

Any particles carried in the ink that are less than 60 microns in diameter will be carried into the nozzle channel 114. Any of these particles which are greater than 20 microns in diameter cannot be ejected from the nozzle 110. Even if pre-filtered ink is supplied to the user, there is a possibility of particle contamination when the ink is re- filled. Therefore, the ink must be effectively filtered to eliminate any particles between 20 and 60 microns.

With regard to power supply, the peak current consumption or the full width colour ZBJ head 200 is about several amperes. This must be supplied to the entire length of the chip 100 with insignificant voltage drop. Also, the ZBJ head has more than 35 signal connections, the exact number depending upon the chosen circuit design, and accordingly insignificant voltage drop is also required.

Mechanical support to the ZBJ chip 100 can be provided by the ink channel extrusion 210 in the manner shown in Fig. 37. The ink channel 210 extrusion has three functions: to provide the ink paths and keep the four colours separate; to provide mechanical support for the ZBJ chip 110; and to assist in dissipating the waste heat to the ink 106.

It is for these reasons it is preferable that the ink channels extrusion 210 be extruded from aluminium, and anodised to provide electrical insulation from the busbars 201 and 202. Manufacturing accuracy of the extrusion 210 need only be maintained to approximately $\leq$ 50 microns, as the extrusion 210 is not in contact with the nozzles 110. The edges of the channel extrusion 210 should be sealed against the ZBJ chip 100 to prevent air from entering the head assembly 200. This can be achieved with the same epoxy as that used to glue the assembly 200.

Fig. 44 illustrates an exploded perspective view of a preferred construction of a high speed full colour ZBJ assembly 200. The filter 205 is preferably a 10 micron (or finer) absolute filter such as a filterite "Duofine" (Trade Mark) bonded fiberglass filter. The surface area of this filter through which the ink must flow is 528 mm^2. With an ink flow rate of 1.28 ml per second, the ink must pass through the filter at a velocity of 2.4 mm per second. If the filter 205 is compressible, it can also farm a gasket to prevent pigment flow between the four colours. In this case, the ZBJ chip 100 can he glued to the extrusion 210 under pressure. Alternatively, a silicone rubber seal can be used. In this case, care must be taken not to contaminate the ink channels 211-214.

One way of supplying the necessary power to the chip 110 is by power connections which run the full length of the chip 110. These can be connected using tape automated bonding (TAB) to the busbars 201 and 202 which form part of the head assembly 200. The signal connections to the ZBJ chip 100 can be formed using th sam TAB tapes as ar used to supply pow r to the ZBJ chip 100. Furth rmor , as in Fig. 4, th busbars 201, 202 can be configured as heat sink l m nts surrounding the extrusion 210.

Ink Drops:

With a fault tolerant design requiring the formation of two separate heater elements 121, 122, the ink drop 108 does not necessarily exit perpendicular to the ZBJ head surface. The ink drop 108 can be deflected by the shock wave of the expanding bubble at different angles depending on whether the main 121 or redundant 122 heater was fired. Such a configuration is illustrated in Figs. 45 and 46 respectively which should be viewed in conjunction with Figs. 10 and 12.

The angle and degree of the deflection 153 and 154 will depend upon the exact geometry of the ZBJ nozzle 110, and the mode of propagation of the bubble's 116 shock wave through the ink 106. The edit angle of the drop 108 is not important in itself. However, any difference between the exit angle of the drop fired by the main heater 121 and one fired by the redundant heater 122 will degrade the image quality slightly. The above can be reduced in two ways:

Firstly by positioning the head 200 closer to the paper 220 to reduce the distance between the two spots on the paper 220, and secondly by delaying the time of the redundant nozzle firing so that the paper movement cancels the deflection angle 153 or 154. This requires that the main and redundant heaters be aligned in the direction of paper movement 222.

Power Supply:

The A4 full width continuous tone ZBJ head 200 has a high current consumption of several amperes when operating. The distribution of this current to and across the chip 100 is not possible using standard integrated circuit construction. However, the geometry of the ZBJ chip 100 leads to a simple solution. The entire edge of the chip 100 can be used to supply power, with connections being made to a wide aluminium trace along both of the long edges of the chip 100. Power can be supplied by the busbars 201 and 202 along both sides of the chip 100 connected to the chip by tape automated bonding (TAB), compressible solder bumps, spring leaf connection to gold plated traces, a large number of wire bonds, or other connection technology.

Fig. 41 illustrates one method of TAB connection along the length of the ZBJ chip 100 with the connections shown in magnified detail. Fig. 48 shows a magnification of an alternate arrangement using a knurled edge for multipoint contacts.

With reference to Fig. 47, the heatsink/busbar (51,52) (201,202) can readily be made larger, or of different shape, or of different materials without affecting the concept of the ZBJ head 200. Forced air, heat pipes or liquid cooling can also be used. It is also possible to reduce the current consumption by reducing the duty cycle of the nozzle 110. This will increase the print time, but reduce the average power consumption. The total energy required to print a page will not be affected.

Power Dissipation:

The full length full colour head can have a power dissipation of up to 500 watts when all nozzles are printing, depending on the nozzle efficiency. Before a final design of a ZBJ head can be derived, the following should be taken into account, as all these factors affect beat generation and dissipation.

(1) The number of nozzles: The number of nozzles 110 directly effects the power dissipation, but is also linked to print speed, image quality and continuous tone issues.

(2) Heater energy: The heater energy is typically 200 nJ per drop. Any reduction in heater energy allows the power dissipation to be reduced without affecting print speed.

(3) Supply Voltage: A low supply voltage is desirable, however, a reduction in voltage increases the current consumption and the size of on-chip driver transistors. Power dissipation will not be greatly affected by the supply voltage if the nozzle energy is maintained constant. In the preferred embodiment a supply voltage of +24V is used for the heater drivers and +5V for logic electronics.

(4) Nozzle Duty Cycle: Increases in the nozzle duty cycle directly increases the power consumption but also increases the print speed.

(5) Print Speed: Print speed is related to the number of nozzles 110, the number of drops per pixel, the pixel size and the nozzle duty cycle. A reduction in print speed can reduce power requirements, but typically will not affect the total energy per page.

(6) Permissible Chip Temperature: The chip temperature must be maintained well below the boiling point of the ink 106 (generally about 100°C).

(7) Ink Channel Geometry: This will affect the amount of heat dissipation available through the ink 106.

(8) Cooling Method: Convection cooling is adequate for scanning heads, but full length heads require additional methods such as heat sinks, forced air cooling or heat pipes. Liquid cooling is a possible solution to the problem of high power density in the head strip. As liquid ink is already in contact with th

h ad, a recirculating pumped ink system with a h at xchang r can be us d if heat dissipation probl ms cannot be solved by easier methods.

(9) Ink Th rmal Conductivity: Th th rmal conductivity of th ink 106 becomes r l vant if th ink is to provid a significant pow r dissipation conduit.

(10) Ink Channel Thermal Conductivity: The thermal conductivity of the ink channel extrusion 210 is also relevant.

(11) Heat Sink Design: Heat sink size and design can be readily changed to provide optimum heat dissipation. The heat sink can be made quite large with little expense and little adverse effect at the system level. This is especially true of the full page versions as the ZBJ head 200 does not move (i.e. the paper moves relative to the head 200).

(12) High Temperatures: The operating temperature of the ZBJ heater elements 121,122 in excess of 300.C. It is important that the active elements (drive transistors and logic) of the ZBJ chip 100 do not experience this temperature extreme. This can be achieved by locating the drive transistors as far from the heater elements 121,122 as possible. The active elements can be located at the edges of the chip 100, leaving only the heaters 120 and the aluminium connecting lines in the high temperature region. Also, obtaining an adequate heat transfer is a serious potential problem. The heater 120 should exceed 300°C yet the overall chip temperature must be kept well below the boiling point (100.C) of the ink 106. While heat transfer from the heat sink (51,52) to ambient should not be a problem, transferring heat from the chip 100 to the heat sink (51,52) efficiently is important.

Heater Drive Circuits

The scanning bubblejet head used in Canon's BJ10 printer has 64 nozzles energised by an array of heaters 6 which are shown in Fig. 49. These are multiplexed into an 8 x 8 array using diodes 8 integrated onto the chip. External drive transistors (not illustrated) are used to control the heaters 6 in eight groups of eight heaters 6.

The prior art approach has several disadvantages for large nozzle arrays. Firstly, all of the heater power must be supplied via the control signals and this can require a large number of relatively high current connections. Also, the number of external connections becomes very large.

The preferred embodiment of the ZBJ chip 100 includes drive transistors and shift registers on the chip 100 itself. This has the following advantages:

- (1) Fault tolerance can be implemented at low cost, with no external circuitry;
- (2) All heater power is supplied by two large connections, V+ and ground with control lines being at signal levels only;
- (3) The number of external connections is small, irrespective of the number of nozzles 110;
- (4) External circuitry is simplified;
- (5) No external drive transistors are required;

and

- (6) There is only one transistor in series with each of the heaters 121,122, instead of two transistors and a diode 8 as with the prior art. This allows a possible reduction in operating voltage.

However, disadvantages of this approach are:

- The ZBJ chip 100 circuit is more complex; and
- More semiconductor manufacturing process steps are required thus reducing the yield.

Fig. 50 shows the logic and drive electronics of the ZBJ chip 100 with 32 parallel drive lines, corresponding to the 32:1 nozzle duty cycle. The enable signals provide the timing sequence, firing each of the 32 banks of nozzles 110 in turn. The enables can be generated on-chip from a clock and reset signal.

In Fig. 50, the Vdd is 15 volts and Vss is tied to a clean ground point. V+ and ground have noise of up to several amperes, so may not be suitable for logic even though they are supplied to the chip 100 at a very low impedance.

Shown in Fig. 50 is a heater driver 124 for two nozzles 110. The drivers 124 consist of two individual drivers 160 and 165 for two nozzles (without fault tolerance) showing the data connections of the shift registers.

Each heater driver 160, 165 consists of four items:

- (1) A shift regist r 161,166, to shift the data to th correct heat r drive. Th shift register 161,166 can b dynamic to reduc th transistor count;
- (2) A low power dual gat nabl transistor 162,167;
- (3) A medium pow r inv rting transist r 163,168. This inv rts and buff rs th signal from th nabl transistor 162,167 and combines with th enabl transistor 162,167 to provid an AND gate; and

- (4) A 1.5 milliamp driv transistor 164,169. The AND function is not incorporated into the drive transistor 164,169 as the capacitance on the enable lines to too large.

For a ZBJ head with 1,024 (32 x 32) nozzles, th clock period is the game as th pulse width, because 32 bits of data must be shifted in ach shift regist r between nozzl firings, and th r is a 32:1 duty cycl . The circuit of Fig. 50 is only suitable for a ZBJ head with less than 1,024 nozzles. However, where there is only a small number of nozzles an active circuit provides little advantage, and a diode matrix can be used.

For larger heads, with more than 1,024 nozzles, the clock required to shift all of the data to the appropriate nozzles requires a period shorter than the heater pulse. For the full width high speed full colour ZBJ head 200 of Fig. 5, 51,200 bits of information must be shifted into the head in 200 microseconds. This requires a clock rate of about 8 MHz. The data at the shift registers 161,166 therefore only need be valid for 125 nS but is required for the full duration of the 6.25 microsecond heater pulse. Disclosed herein are two solutions to this problem, one being a transfer register and the other being clock pauses.

Fig. 51 illustrates the addition of a transfer register 172 to a main heater drive 170 having componentry otherwise corresponding to that of Fig. 50. This arrangement provides a simple solution to the above problem but has the disadvantage of increasing the amount of circuitry on the chip 100. 1,600 bits of data are shifted into each shift register 171 at 8 MHz. When the enable pulse occurs, the data is parallel loaded to the transfer register 172 where it is stable for the duration of the heater pulse.

An alternative which avoids the extra transistors of the transfer register 172 is to introduce pauses into the clock stream for the duration of the heater pulse, so that the data does not change during the pulse. This is illustrated in Fig. 52 and in this case, the 1,600 bits of data are shifted into the register at a slightly higher rate - 8.258 MHz -after which there is a pause in the clock for 6.25 microseconds, the period of heater pulse. Each of the 32 rows of heaters fire at different times. The clocks for each row can be simply generating by gating the constant 8.258 MHz clock with the heater enable pulses.

Fig. 53 illustrates one stage of a ZBJ drive circuit 177 which incorporates clock pauses. An AND gate 178 connects between the clock and Enable lines and drives the CLK inputs of the shift registers 161 (and 166 not illustrated but connected at 179).

This approach has the disadvantage of requiring relative complex data timing on the chip 100. However, this can be supplied at low cost by the custom designing of ZBJ data phasing chips 310 such as those shown in Fig. 56 (to be later described).

Long Clock Lines:

For the full length colour ZBJ head 200 having 51,200 nozzles, with full redundancy, there are 102,400 shift register stages distributed over a length of 220 mm. These are structured as 64 shift registers each with 1,600 stages. Transmission line effects and the large fanout necessary preclude the clock from being driven by a single line. Fortunately, the clock can be regenerated at short intervals. If the clock is regenerated 32 times, each clock segment will have a fanout of 50, and will be only 6.8 mm long.

In Fig. 54, a simple clock regeneration scheme 180 is shown including a chain of shift registers 181 each supplying a corresponding heater driver 124. Included in the clock line are Schmitt triggers 182 equally spaced depending on the permissible fanout. As seen, where a Schmitt trigger 182 occurs in the chain, the next corresponding shift register 181 is input not from the shift register 181 immediately preceding it in the chain, but from the one before that. This compensates for the delay imposed by the Schmitt trigger 182.

Clock regeneration is degraded by the introduction of a propagation delay (T_{PD}) at every regeneration stage. If the propagation delay of each regenerator is substantially less than the clock period, the ZBJ circuit will still function. This is because the data of each stage of shift register 181 will also be delayed by T_{PD} every time a regenerated clock is encountered. Therefore, the valid data window will not change. With an 8 MHz clock, T_{PD} must be less than 125 nS and greater than the propagation delay of the shift register. This can be readily achieved.

Any digital circuit will have a difference between rise and fall times (T_{PLH}-T_{PHL}). In a 2 micron NMOS ZBJ circuit, these times will be quite large, due to the high capacity load and passive pull-up on the clock regenerator outputs. A T_{PLH}-T_{PHL} value of 5 nS is a reasonable assumption. Under these conditions, the clock pulse will disappear after only thirteen stages of regeneration. A solution is to regenerate the pulse width with a monostable at v ry stag , as shown in Fig. 55, which ss ntially corresponds to Fig. 54 save for th insertion of a monostabl 183 aft r each Schmitt trigger 182 in th clock lin .

Th actual pulse width g nerated by th monostables 183 is not critical. It must be long r than th minimum pulse width required by th shift registers 181 (about 10 nS), and short r than th clock period (125 nS). This tolerance is important to allow for th inaccuracy of component values in monolithic circuits.

Ext rnal Driv r Circuit

Th full colour ZBJ head 200 requir s a data rate of 32 MByt s p r second (8 MHz av rag clock rate x 32 bits). This data must be d layed by up to 7,600 microseconds, and requir s nearly 1 megabit of d lay storage. If the clock pause system described earlier (Fig. 53) is used to reduce the logic on the ZBJ chip 100, then data must also be presented to the ZBJ chip 100 with a complex timing scheme.

Fig. 56 is a block diagram of an overall data driving scheme for the full colour ZBJ head 200 in which an image data generator 300, such as a computer, copier or other image processing system, outputs colour pixel image data on a 32 bit bus 301. The colour pixel image data is normally supplied in raster format (cyan, magenta, yellow and black (CMYK)) with components for each colour being provided simultaneously on the bus 301. Because it is not possible for the nozzles for each colour to sit one on top of the other for simultaneous printing, the different colour data must be appropriately delayed prior to being supplied to the head 200. The colour data produced by the computer 300 on the bus 301 is digital data at 1600 dpi with pre-calculated screen or dithering simulating 400 dpi continuous tone colour image.

The bus 301 is divided into blocks of its component colours (cyan, magenta, yellow and black) each of which is respectively input to the ZBJ head 200. The magenta, yellow and black data are delayed by respective line 303, 304 and 305 because these colours are printed sequentially after cyan for each pixel across the head 200. An address generator 302 is used to sequence colour data through the line delays 303- 305. A clock 306 of 8,258 MHz is used to sequence all pixel data and is also supplied to the head 200, which also has a number of power connections 307 as illustrated.

The 10, 20 and 30 line delays are formed using three standard 64 K x 8 SRAMs with a read/modify/write cycle time of less than 120 nS. This is achieved by reading and then writing the SRAMs with the data, while incrementing the address modulo 16,000, 32,000 and 48,000 respectively. The address generator 302 is a simple modulo 16,000 counter, with the two most significant bits of the address of each SRAM generated separately.

Because of the staggered configuration of the nozzles 110 for each array, as seen in Fig. 43, the delays to each data line are different. Generally the provision of these delays requires a large number of standard chips. For this reason, a ZBJ data phaser ASIC 310 is provided to buffer each nozzle array input so as to reduce system complexity. A single ASIC can be constructed which can be used to provide delays for the 8 bits of any of the four colours.

Fig. 57 illustrates a block diagram of a data phaser 310 suitable for the nozzle arrangement in the four nozzle per colour example earlier described. If other nozzle arrangements are used, the length of the delays must be altered to suit. The 50 clock delays 314,315,316 are selectable via a colour select input 313 and are included to allow the same chip 310 to be used for any of the four colour components. The colour select 313 operates a multiplexor which can select data output from any one of the delays 314-316 or directly from the data input 312.

The ASIC 310 of Fig. 57 has a very simple design, but requires around 56 Kbits of data storage. It is therefore most suited to standard cell or data-path compilation techniques.

The data connections 327 to the ZBJ head relate to the firing order, which determines the length of the delay required. Here, the firing order can be determined by adding the number specified to "c" representing colour (black = 0, yellow = 1, magenta = 2, and cyan = 3).

An enable pulse generator 326 provides enable pulses for the heater drivers 124 (previously described).

ZBJ Head Cost:

For full colour full length ZBJ heads to be applicable to large markets, such as colour photocopies and printers selling for less than about USS5,000, the manufacturing cost of the head should as low as possible. In general, a target assumed for each head is about USS100 or less in volume with a mature process.

The ZBJ head 200 is essentially a single piece construction and the head cost will consist almost entirely of the ZBJ chip 100 itself. The ZBJ chip 100 cost is determined by processing cost per wafer, number of heads per wafer, and yield. Assuming that the processing costs per wafer is about S800, and the number of head per wafer is 25, the pre-yield cost per head is S32.

To achieve a head cost of S100, the mature-process yield must be about 30%. However, the chip area for th full colour full length ZBJ heads 200 is of th ord r of 8.8 cm^2. Those skilled in th art would initially b li v that such a larg siz would imply a yield close to zero. Howev r, th re ar sev ral factors which mak th xpectant yield not as low as first impressions. Those factors are:

- (1) Most of th chip 100 c nsists of heaters, nozzl tips, and connecting lin s, which should not b sensitiv to point dislocations in th silicon waf r;

- (2) The majority of th chip 100 has a three micron or gr at r f atur size, and will be r latively insensitive to very small particl s;
- (3) Th chips 100 are not subject t semiconductor proc ssing st ps in ar as lik ly to be affect d by wafer-etch rounding, r sist-edg beading, or process shadowing (i. . th r ar no activ circuit lem nts near the nozzles).

The fault tolerance redundancy of the ZBJ head is preferably provided to improve the yield. This can allow a large number of defects to exist on the chip without affecting the operation of any of the nozzles. Furthermore, it is not necessary to incorporate 100% redundancy, but it is necessary to reduce the non-redundant region of the ZBJ head to a size consistent with an adequate yield. The effect of fault tolerance on yield is discussed later in this specification. Even with fault tolerance, there are several factors which can act to reduce yields below reasonable levels. Some of these factors are:

- (1) Process variations whereby large area variations in process parameters such as etch depth and sheet resistance beyond acceptable limits will result in no yield from affected wafers. Generally, tolerances on these parameters are matched to the ZBJ head requirements during production engineering;
- (2) Mechanical damages: if the mechanical strength of any ZBJ head design is adequate to withstand processing stresses, the ZBJ design can be altered to provide adequate strength. However, this alteration is normally at the expense of the chip area, and therefore yield;
- (3) Wafer taper: the ZBJ chip 100 is unusually sensitive to wafer taper due to the back-etching of the nozzles 110. Wafers should be polished to reduce taper to less than 5 microns before processing;
- (4) Slip: as the chips 100 extend the entire length of the wafer, major slip defects can reduce yield to zero. A special furnace design and processing can be provided to accommodate the long rectangular wafers;
- (5) Etch depth: this must be consistent to within 5% over the entire wafer to ensure that the barrel plasma etch does not etch the heater. If this tolerance is unable to be achieved, the particular ZBJ design should be altered to be less sensitive to etch variations.

Fault Tolerance

As indicated earlier, fault tolerance is included in the ZBJ chip 100 so as to improve yield as well as to improve head life. The provision of fault tolerance is considered essential so as to achieve low manufacturing costs of the ZBJ chips 100. Furthermore, whilst the fault tolerance concept described herein is specifically applied to the ZBJ chip 100, the same concept can be used for other types of BJ heads if a configuration with two heaters per nozzle is created.

The disadvantage of fault tolerance is that chip complexity is doubled. However, due to the topography of the nozzles 110, there is only a slight (about 10%) increase in chip area. The yield decrease this causes is dwarfed by the yield increase provided by fault tolerance.

The ZBJ system described herein implements fault tolerance by providing two heater elements 121,122 for each nozzle 110. As the nozzles 110 are circular and on the surface of the chip 100, each heater 120 is provided with two heater elements 121,122 on opposite sides of the nozzle 110 and preferably having identical geometries. The heater elements are termed a main heater 121 and a redundant heater 122, as seen in Figs. 58A and 58B, although the configuration of Fig. 13 can also be used. Accordingly, the ink drop fired from the nozzle tip 111 by either heater 121 or 122 is essentially the same.

Control of the redundant heater 122 for fault tolerance is provided by sensing the voltage at the drive transistor to the main heater 121 drive. This node makes a high-to-low transition every time the nozzle 110 is fired. Three faults are detected by the behaviour of this node:

1. Open heater: if the heater 121 is open circuit, the node will be stuck low;
2. Open drive transistor: if this occurs, the node will be stuck high; and
3. Shorted drive transistor: if the transistor is short, the heater will overheat, go open circuit and the node will be stuck low.

Fig. 59 illustrates a drive circuit 185,186 for one nozzle of the ZBJ chip 100 with fault tolerance implemented as a digital circuit sampling at the drain of the main heater 121 driver transistor 164.

A latch 189 stores the fault condition detected by the node being low when the heater 121 drive is off. Th latch 189 outputs to an AND gate 191 which is also supplied with th driv signal of the main h at r 121 drive transistor 164, to indicat that th heater 121 should b on. Another AND gat 190 detects th open drive transistor condition. Th tw AND gat s 190,191 ar input to an OR gat 192 to control the r dundant h at r 122.

Becaus the pulse width and v ltag of an operational circuit is stable to within narrow bounds, it is

possibl to r plac the digital circuit of Fig. 59 with a simpler analog circuit, such as that indicated in Fig. 60. In this arrangement, a capacitor 194 and diodes 196 generat a pulse whenev r th high-to-low transition of an operational circuit occurs. This pulse inhibits the firing of th redundant heat r 122 wh n th main h at r 121 circuit is operational. If th main h ater 121 fails, th n th redundant heat r 122 will fir at the times that the main heater 121 would have fired.

Component values are chosen to ensure that the pulse is longer than the heater-on time (6 microseconds) but shorter than the pulse repetition time (200 microseconds). This permits substantial component tolerance.

The heaters 121 and 122, the drive transistors 164,193 and associated connections will consume more than 90% of the area of the ZBJ chip 110, so as a substantial degree of fault tolerance can be provided by providing redundancy in just these areas. However, protection is only provided against small area defects. Any defects with a diameter greater than approximately 10 microns will cause failure.

Fault tolerance can be readily extended to include 100% redundancy of the electronics of the ZBJ chip 100. At the same time, tolerance of some faults from defects of up to 600 microns in diameter can be introduced. This is achieved by duplicating the shift registers 181 described earlier, as well as the drive circuitry. As the shift registers 181 do not consume a substantial amount of chip area, the cost increase of this duplication is exceeded by cost decrease from yield improvement.

Fig. 61 shows one stage of a ZBJ drive circuit with complete redundancy in which the main drive circuit 187 is duplicated, but with the addition of a circuit (resistor 250 and capacitor 199) which inhibits the firing of the redundant circuit 188 when the main circuit 187 is operational.

Fig. 62 shows a simple chip layout of a small length of the ZBJ chip 100, to provide wide area fault tolerance. While large area faults in drive circuitry can be corrected, only small area faults can be corrected in the nozzle area. This is because the main and redundant heaters 121 and 122 must be in the same nozzle 110. However, the nozzle area has no active circuitry and will not be sensitive to faults in most mask layers.

A defect which happens to break the shift register chain of either the main circuit or of the redundant circuit, will mean that subsequent driver stages will not be fault tolerant. Also, a stuck-high fault in the data sequence of either the main or redundant shift register will result in chip failure, as will a Vss to Vdd short. However, these types of faults represent only a small percentage of possible faults.

Placement of the main 156,158 and redundant 157,159 circuits on opposite edges of the chip 100 as seen in Fig. 62 introduces a problem when used in the circuit of Fig. 61. The problem is that the power wiring to the redundant drive transistor 193 must loop across the chip 100, in the manner as shown in Fig. 63. Thin loop can consume substantial chip area, as it doubles the total number of high current tracks across the chip. This can be corrected by reversing the series connection of the redundant heater 122 and redundant drive transistor 193. This requires the introduction of a level translator 257 to control the redundant drive transistor 193. This is illustrated in Fig. 64 which shows one stage of a ZBJ drive circuit designed for large-area fault tolerance.

Approximately 50% of the surface of the chip 100 is covered by aluminium connections between the drive transistors 164,193 and the heaters 121,122. As these interconnects use a fine line width, defects are highly probable. Table 2 lists possible fault conditions and their consequences, assuming that there is only one defect in the affected head circuit.

Each of the conditions indicated in Table 2 are fault tolerant, except where the two main drive tracks are shorted. This can be made fault tolerant by incorporating a fuse between each main drive transistor 164 and its heater 121. However, the fuse must he highly accurate and must "blow" at twice the heater current but not one times the heater current. A more elegant solution is to interleave the main drive tracks with the redundant drive tracks. This configuration increases the defect size required to short two main drive tracks by a factor of 3. Such an arrangement reduces the defect density for this source by a factor of 9.

The foregoing arrangements to provide fault tolerance occur at a nozzle level through duplication of the heaters 120. However, this does not ensure correct operation if, say, a nozzle 110 becomes blocked. Where this occurs it is necessary to provide fault tolerance at a chip level through the duplication of nozzle arrays such as shown in Fig. 65.

Here a redundant nozzle ZBJ chip 450 is shown having a main cyan nozzle array 451, a redundant cyan nozzle array 452, and a similar configuration for each of magenta (453,458), yellow (455,456) and black (457,458). In this configuration, should a nozzl in th main array fail, a corr sponding nozzl in th redundant array fir s. This is furth r d picted in Fig. 65 wher a main cyan nozzle 451A is fired by a h ater 461 nergized through a switch 460 and a redundant cyan nozzle 452A is fired by a similar heater 463 and switch 462. Interconnecting th switches 461 and 462 is a fault d t ctor 464 which senses a fault in the main cyan nozzle 451A and provid s a firing pulse to the switch 462. Becaus of th physical displacem nt

of th array 452 with r spect to th array 451, it is nec ssary to compensat for tim and/or motion f th relative mov m nt of the paper across the chip 450. This is provided by a parallel loading shift regist r 465 which detects all of the faults occurring in one row of nozzl s and shifts th data out as a serial data str am. This data is th n delayed by an appropriate number of lin d lays and placed in a serial to parallel shift register, where it causes the actuation of the redundant heater 463 via the redundant switch 462.

System level fault tolerance can be provided in the manner shown in Fig. 67 where two thermal ink jet chips 470 and 475 are arranged side-by-side. The chip 470 acts as a main device with the chip 475 acting as a redundant device thereby the arrays 471-474 being compensated by the arrays 476-479 in the manner described above. However, with this configuration each nozzle 480 must connect to it's corresponding nozzle 481 using a fault detector 482 and compensator 483 as before. This can be achieved by shifting the fault data off the main chip 470, delaying it, and using that data to fire the nozzles of the redundant chip 475.

Dicing and Handling

Because the ZBJ chip 100 is very long and thin, and has many holes etched through it, the mechanical strength of the chip 100 is insufficient to allow high yield dicing in the conventional manner.

A simple solution using a diced back etch is illustrated in Fig. 68 where channels 147 are etched in the back surface of the wafer 149, most of the way through the wafer 149. The wafer 149 is then scored 145 on the front surface. The channels 147 can be etched using the same processes that are used to etch the ink channels 101 and nozzle vias 110. The spacing of vias 146 along the dice line 145 can be adjusted to give the optimum trade-off between strength for handling and ease of dicing. To prevent the ZBJ chips 100 from accidentally separating during the remaining processing steps, tags 148 (Fig. 46) can be left along the edges of the wafers 149. These tags 148 must be diced off before the ZBJ chips 100 are separated. If the tags 148 are, say, 5 mm wide, then the wafer length for 220 mm heads must be 230 mm. The wafers 149 can also be supported by these tags 148 during the various chemical processing steps to prevent processing "shadows" from affecting the regions of the ZBJ chip 100.

Lithography

The full width colour ZBJ chip 110 has dimensions of approximately 220 mm x 4 mm, yet requires very fine line widths, such as 3 microns for the one nozzle per pixel design, and 2 microns for the four nozzle per pixel design. The maintain focus and resolution when imaging the resist patterns is difficult, but is within the limits of current technology.

Either full wafer projection printing or an optical stepper can be used. In both cases, the projection equipment requires modification to the stage to allow for 220 mm travel in the long axis.

In a 1:1 projection printing system, a scanning projection printer is modified to match the mask transport mechanism to permit very long masks. Defects caused by particles on the mask are projected at a 1:1 ratio and are in focus, so cleaner conditions are required to achieve the same defect level. A 1:1 projection printer also requires a mask of an image area of 220 mm x 104 mm. This requires modification to the mask fabrication process. The manufacturing of 2 micron resolution masks of this size is viable for high volume production, but the masks are very expensive in small volumes. For these reasons, a stepper configuration should also be considered.

The use of 5:1 reduction stepper reduces some of the problems associated with a scanning projection printer, particularly those associated with the production of very large masks, and the particle contamination of the mask. However, some new problems are introduced. Firstly, a different imaging area of 10 mm x 8 mm is used. Then the full size wafer can be imaged in 22 x 13 steps. This provides a total of 286 steps which generally takes about 250 seconds to print. As there are approximately 10 imaging steps required for the manufacture of the ZBJ chip 100, total exposure time per wafer can be about 2,500 seconds which substantially reduces the production rate of such devices. Also, the use of the wafer stepper introduces the following two problems which effect the ZBJ chip design:

1. The ZBJ chip 100 is longer than the step size in one axis; and
2. The mask cannot readily be changed during exposure of the wafer, therefore one mask must be used for the ntir h ad.

The first of these probl ms can be count red by using a r peating d sign, and nsuring that alignm nt at the perimeters of that r peating block is not critical. As th wafer 149, is only dic d in on direction, th repeating block does not hav to be rectangular, but can avoid critical f atur s such as nozzl s. Th l ft hand and right hand edg s of the mask patt rn can be quit irregular, provided they match ach oth r.

Also, each signal lin must t rminat at th bonding pads 207,223, which ar typically arranged at the side edges of th chip 100. This normally requires that the side edges of th chip 100 be imaged with a differ nt pattern than that of th centr of th ZBJ chip 100. This can be achi ved by blading the mask to obscur th bonding pads and associated circuitry on all but th first xposur of th chip.

Fig. 70 shows a basic floor plan or chip layout of a stepper mask for a full width continuous tone colour ZBJ chip 100, including complete redundancy for full fault tolerance. The magnified portion of the drawing illustrates an irregular mask boundary 258.

ZBJ Production Process:

The ZBJ chips 100 can be processed in a manner very similar to standard semiconductor processing. There are however, some extra processing steps required. These are: accurate wafer thickness control, deposition of a HfB_2 heater element; etching of the nozzle tip; back etching of the ink channels; and back etching of the nozzle barrels.

A 2 micron NMOS process with two level metal is assumed as this is the basis of the four nozzle per pixel design. CMOS or bipolar processes can also be used.

Wafer preparation for scanning BJ heads is similar to that for standard semiconductor devices, except that the back surface must also be accurately ground and polished, and wafer thickness maintained at better than 5 microns. This is because both sides of the wafer are photolithographically processed, and etch depth from the reverse side is critical.

Full width fixed ZBJ chips require different wafer preparation than do those used in scanning heads, as the ZBJ chip must be at least 210 mm long in order to be able to print an A4 page, and at least 297 mm long for a A3 pages. This is much wider than the typical silicon crystalline cylinder. Wafers can be sliced longitudinally from the cylinder to accommodate the long chips required.

When the wafer has been ground and polished the resultant wafer should generally be about 600 microns thick. The resultant wafer is a rectangular shape approximately 230 mm x 104 mm x 600 microns thick. On this wafer, approximately 25 full colour heads can be processed. Such a wafer will appear similar to that of Fig. 69. A 230 mm long 6 inch cylinder can be used to produce up to 2,600 full width, full colour heads before yield losses.

Due to the one piece construction of the ZBJ print chip 100, and the use of a stepper for exposure, wafer flatness requirements are no more severe than those of the transistor fabrication processes. The wafer can be gettered using back-side phosphorous diffusion, but back-side damage can result and therefore is not recommended because the back-side is subsequently etched.

Wafer processing of the ZBJ chip 100 uses a combination of special processes required for heater deposition and nozzle formations, and standard processes used for drive electronics fabrication. As the size of the ZBJ chip 100 is largely determined by the nozzles 110 and not by the drive transistors 164,193, there is little size advantage in using a very fine process. The process disclosed here is based on a 2 micron self-aligned polysilicon gate NMOS process, but other processes such as CMOS or bipolar can be used. The process size disclosed here is the largest size compatible with the interconnect density required to the nozzles 113 of the high density four colour ZBJ head. This also requires two levels of metal. Two levels of metal can be required for simpler heads, as high current tracks run across the chip, and very long clock tracks run along the chip.

The wafer processing stops required for the formation of the ZBJ nozzles 110 are intermingled with the steps required for the drive transistors. As the process used for the drive transistors can be standard as known to those skilled in the art, there is no requirement to specify such steps in this specification.

The wafer processing of the ZBJ chip 100 is illustrated in Figs. 71 to 80 which show the cross section for a single nozzle corresponding to the cross-sectional lines shown in Fig. 12. Figs. 71 to 80 also illustrate the corresponding and simultaneous construction of transistors arranged outboard of the nozzle arrays.

Firstly, with reference to Fig. 71, a 0.5 micron layer 132 of thermal SiO_2 is grown on the P-type doped substrate 130. This is patterned with the driver circuit requirements as well as with the thermal shunt vias 400.

With reference now to Fig. 72, a thin gate oxide is thermally grown on the substrate 130. This will also affect the electrical connections of the thermal shunt 140 to the substrate 130, but will have an insignificant ffect on th rmal conduction. P lysilicon is d posited to form th gates 403 and int rconnects of th transistors. Th drain and source of th transistors ar N-type doped using the polysilicon gat 403 as a mask. This will also dope th th rmal shunt connection 403 to th substrat 130. A 0.05 micron layer of HfB_2 is deposited to form th heat r 120. A 0.5 micron lay r of aluminium is d posited ov r th substrat 130 to form th first lev l of metal 134. A resist is patterned with th sum of th h at r and th first l v l

m tal 134, and w t tched with a phosphoric acid-nitrat tchant. Th HfB_2 lay r is r active ion tched using the aluminium as a mask. The etch is performed with a halog nic gas such as CCl_4 (carbon t trachloride), as d scribed in US Patent No. 4,889,587. Th wafer is th n at th stag illustrated in Fig. 72. Th mask shows th ground common track 405 and th V+ common track 405.

A resist is then patterned with a pattern which exposes the heater element 120, and wet etched with a phosphoric acid-nitric etchant. The wafer then corresponds to that illustrated in Fig. 73, also showing a heater connection electrode 407, and HfB_2 408 under aluminium.

If the above steps are followed, there will result a 500 Angstroms layer of HfB_2 under all of the first level of metal 134. This includes the connections to the sources and the drains of all the FET'S as well as Schottky diodes, in the control circuitry. If necessary, another masking and RIE etching can be used before the deposition of aluminium to remove HfB_2 from unwanted areas.

Fig. 74 illustrates the provision of the interlevel oxide 136. This is layer of CVD SiO_2 or PECVD SiO_2, approximately 1 micron thick. The thickness of this layer can be determined by the thermal lag required between the heater 120 and the thermal shunt 140. Fig. 74 shows the cross-section of the water after this step in which 410 is a thermal shunt via, 411 represents the nozzle cavity, 412 a via for connection to the transistor and 413 the heater connection vias.

Referring now to Fig. 75, the second level metal 138 is formed as a layer of 0.5 micron aluminium which forms both the thermal shunt 140 and the second level of interconnects 144 to the heaters 120, heater connection 416 and connection 415 for the drive circuitry. Two levels of metal are unlikely to be necessary for ZBJ heads with one nozzle per pixel, but are likely to be required for high speed colour heads with four nozzles per pixel. The thickness and material of this layer can be changed to suit the thermal requirements of the heater chamber depending on the specific application.

Referring now to Fig. 76, a CVD glass overcoat 142 is applied, approximately 4 microns thick. A low temperature CVD process, such as PECVD, can be used. This layer is very thick and provides mechanical strength for the nozzle tip 417, as well as environmental protection. A 17 micron diameter hole is RIE etched through the 4 micron glass overcoat with an SiO_2 etching species. This forms the top of the nozzle tip 417 and completes the configuration illustrated in Fig. 76.

The hole (417) formed by a RIE of SiO_2 is extended at least 30 microns into the silicon by further RIE, using a silicon etching gas. In this case, the SiO_2 overcoat is used as the RTE mask. As RIE is relatively unselective, a substantial amount of the SiO_2 overcoat will be sacrificed. For example, if the etch rate is 5:1 ($Si:SiO_2$), then the CVD glass overcoat is deposited to a depth of 10 microns so that 4 microns remains after etching the silicon. This hole (417) can be etched as deeply as possible to minimise accuracy requirements in the depth of back etching of the nozzle barrel (113). Reactive ion etching is used to obtain near vertical side walls, to ensure that the ink flows to the end of the nozzle by surface tension.

The wafer is back-etched to a thickness of approximately 200 microns. The actual thickness is not critical, but the variation in thickness is, however. The wafer must be etched such that the thickness variation is less than ± 2 microns over the wafer. If this is not achieved, it is difficult to subsequently ensure that the process of back etching the nozzles does not over-etch and destroy the heaters.

The next step for a four colour head is to RIE etch ink channels 101 in the reverse side of the surface of the chip 100 in the manner illustrated in Figs. 6 to 9. These channels 101 (Fig. 5) are approximately 600 microns wide x 100 microns deep. These channels 101 are not essential to the operation of the ZBJ chip 100, but have two advantages. Namely, the channels 101 reduce the ink flow rate through the filter from approximately 8 mm per second to 2 mm per second. This flow rate reduction can alternatively be achieved by locating the filter differently in the ZBJ head 200. Also, the channels reduce the depth that the nozzles 110 need to be etched from 190 microns to 90 microns. As the nozzle barrels 113 are 40 microns in diameter, this has a major effect on the ratio of length to diameter of the barrels 113.

However, the ink channel back etch 420 has the disadvantage of weakening the wafer substantially. This step can be omitted if desired.

The ink channel back-etching process can also be used to thin the wafer along the dice lines in the manner earlier described with reference to Fig. 68.

The etch depth of the next step, nozzle barrel back- etching 419, is critical to ensure that the nozzle barrel 113 properly joins with the nozzle tip 417 (111) to form the thermal chamber. A solution to this problem is to incorporate end point detection using optical spectroscopy. A chemical etch stop signal can be cr ated by filling the nozzl tips 417 pr viously tched from th front surface of th substrate with a d tectable ch mical signatur , and monitoring th xhaust gases with an emission spectroscope. The nozzl barr ls 113 ar formed with an anisotropic reactiv ion etch of silicon. Holes 40 microns in diam t r (lat r wid ned to 60 microns with an isotropic plasma tch), ar tched 70 microns into th silicon from th r verse side of th wafer. Th se holes ar at th bottom of th pr viously tched ink channels, which ar

100 microns deep. As the wafer is thinned to 200 microns, these holes etch to within 30 microns of the front surface of the silicon.

When the end point 421 detection signal from the spectroscope begins, the etch can be stopped, even if some of the nozzles have not joined up to the tips. This is because the next step (10 micron isotropic etching of all exposed silicon) joins up any that are within about 12 microns. Fig. 77 shows the ZBJ chip at the end of this step.

Etch depth uniformity over the entire wafer surface is critical. The tolerance depends largely upon the depth of each etch achievable with the 18 micron hole etched from the front of the chip. Given that the front etched hole is etched 30 ± 2 microns, wafer thickness is 200 ± 2 microns, ink channel back etch depth is 100 ± 4 microns, overall isotropic etch of silicon is 10 ± 1 microns, maximum joining distance is 12 microns, and the minimum between the nozzle barrel and the heater is 10 microns, cumulative tolerances mean that the nozzle barrel etch must be 70 ± 4 microns. All of these tolerances can be loosened if the front etch can be deeper than 30 microns. The accuracy of alignment of the back-etching process to the front surface processes need only be to within ± 10 microns, as alignment of the barrel and tip is not critical.

The cumulative effect of these tolerances is illustrated in Fig. 78. The cross-hatched area 424 seen in Fig. 78 shows the region of uncertainty in the final nozzle geometry, and the single-hatched area 423 shows the safety margin for the nozzle barrel to nozzle tip join using these tolerances. This safety margin is required because the reactive ion etches will not leave perfectly flat bottomed holes. The uncertainty of the wafer thickness (200 ± 2 microns) and the channel etch (100 ± 4 microns) are combined into one thickness figure of 100 ± 6 microns as the channels are too large to be shown in this figure.

Other minor problems exist with this step, including: the resist must be very thick to be maintained for 70 microns of RIE; the etch is deep and narrow, giving problems with removal of spent etchant; shadowing of the projection pattern by the walls of the ink channels must be avoided; and adequate resist coverage of the stepped surface must be achieved. This is not critical as etching of the ink channel walls can be tolerated.

However, the actual shape and dimensions of the rearside of the nozzles 110 is not critical. This provides considerable scope for other solutions. All that is required is that the minimum mechanical strength is maintained, and that a shape conducive to ink capillary action is achieved. Some possible alternatives are:

- Multi-stage RIE with progressively narrower barrels 113 can be used. This avoids the problems of an accumulation of spent etchant and thick resists, but involves more processing steps;
- Etching of wide holes which encompass several nozzles 110, with the nozzles clustered in groups to provide maximum spacing between these holes, and therefore conserving mechanical strength. This is illustrated in Fig. 81.

The entire ZBJ wafer is then subjected to a 10 ± 1 micron isotropic plasma etch of all exposed silicon. This has two purposes. Firstly, this forms the thermal chamber 115 by undercutting 425 the thermal silicon dioxide 132 in the region of the heater 120. This is also to ensure that the nozzle barrels 113 join with the nozzle tips 111 resulting from a widening 426 of the barrels 113. As the wafer is etched from both sides, any non-joining barrels 113 and tips 111 that are within 18 microns (twice (10-1) microns) should join up. Non-joining barrels and tips within approximately 12 microns will behave essentially similarly to joined barrels and tips. This reduces the accuracy requirements of the barrel back-etch 419.

The etch must be highly selective towards silicon, and have a negligible etch rate with thermal silicon dioxide, otherwise the heater insulation layer 132 will be destroyed. This results in the configuration illustrated in Fig. 79.

The 4 micron glass overcoat 142 must now be etched to expose the bonding pads. This is not performed before the nozzle tip silicon etch because poor selectivity can cause the 30 micron RIE silicon etch to etch through the aluminium layer 139. The ZBJ chip 100 can then be passivated with a 0.5 micron layer 144 of tantalum or other suitable material. It can be difficult to achieve a highly conformal coating, but irregularities in the passivation thickness will not substantially affect the performance of the ZBJ chip 100.

The ZBJ chip 100 has no electrical output, and therefore true functional testing can only be achieved by loading the device with ink into printing and printing patterns which exercise each individual nozzle 110. This cannot be performed at multi-probe time. An effective method of functional testing the chips 100 at multi-probe time is to test the power consumption in the V+ to ground path as each heater 120 is turned on in sequence. Each time a heater 120 is fired, a current pulse should occur. As this is a separate circuit with negligible quiescent current, these pulses are readily detected. The entire pattern of operational heaters and redundant circuits can be determined in approximately 1 second with inexpensive equipment. Therefore the entire wafer can be multi-probed in under one minute. The pattern of functional and non-functional heaters can be read into a computer and used for compiling process statistics and detecting local quality control

problems.

Scribing is along th top surface at the etched dice channels 147 (see Fig. 68). Th end tabs 148 for handling must be diced off befor th ZBJ chips 100 can be separat d. Th chips 100 can be glu d in place in th head assembli s 200 and c nnected using tape automated bonding, with on tape along ach edge of the chip. Alternatively, standard wire bonding can be used, as long as enough wires are bonded to meet the high current requirements of the chip 100. Fig. 80 illustrates the cross-section of the completed device.

Fig. 82 is a plan view of typical components used in a ZBJ chip of the structure shown in Fig. 18. Figs. 83 to 113 are vertical cross-sections through the centre line of Fig. 82 at various manufacturing stages.

Fig. 83: The manufacturing process commences with a standard silicon wafer of P-type doping with a resistivity of approximately 25 ohm cm.

Fig. 84: A layer of silicon nitride 501 approximately 0.15 microns thick is grown on the wafer 500. This is a standard NMOS process .

Fig. 85: A first mask 501 is used to pattern the silicon nitride 501 to prepare for boron implantation.

Fig. 86: The wafer 500 is implanted with a field 503 of boron to eliminate the formation of spurious transistors.

Fig. 87: A thermal oxide layer 504 approximately 0.8 microns thick is grown on the boron implanted field 503.

Fig. 88: The remaining silicon nitride 501 is removed.

Fig. 89: This is a standard NMOS process which implants arsenic to form regions 505 for deletion mode transistors. This step involves the spin deposition of a resist, exposure of the resist to the second mask, development of the resist, arsenic implantation, and resist removal.

Fig. 90: A 0.1 micron gate oxide 506 is thermally grown. This is part of a standard NMOS process and increases the field oxide thickness to 0.9 microns.

Fig. 91: A 1 micron layer of polysilicon 507 is deposited over the entire wafer 500 using chemical vapour deposition.

Fig. 92: The polysilicon 507 is patterned using a third mask 508. The wafer 500 is spin coated with resist. The resist is exposed using the third mask and developed. The polysilicon 507 is then etched using an anisotropic ion enhanced etching to reduce undercutting.

Fig. 93: The gate oxide 506 is etched where exposed by the polysilicon etch of the third mask. This results in etch diffusion windows 509 being formed and will also thin the field oxide 504 leaving a thickness of 0.8 microns.

Fig. 94: N+ diffusion regions 510 approximately 1 micron deep are formed in the diffusion windows 509.

Fig. 95: A 1 micron layer of glass 511 is deposited using chemical vapour deposition.

Fig. 96: The CVD glass 511 is etched where contacts are required to the polysilicon 507, the diffusions 510 and in the heater region. Contact regions 512 are formed. This process differs from the standard NMOS process in that the depth of etch is controlled so that there is an appropriate amount of thermal SiO_2 504 remaining under the heaters.

Fig. 97: A 0.05 micron layer 513 of HfB_2 is deposited over the wafer 500. This is not a standard NMOS process.

Fig. 98: A HfB_2 layer 513 is etched using ion enhanced etching with CCl_4 as the etchant. This exposes the heaters 514. This step requires spin coating of resist, exposure to a fifth level mask, development at resist, ion enhanced etching, and resist stripping.

Fig. 99: A 1 micron first metal level 515 of aluminium is evaporated over the wafer 500.

Fig. 100: The first metal level 515 is etched using a sixth level mask. This step requires spin coating of resist, exposure to the sixth mask, development of resist, plasma etching, and resist stripping. The etch must be strongly selective over HfB_2, as the HfB_2 layer is only 0.05 microns and will be exposed when the metal 515 is etched.

Fig. 101: A 1 micron layers 516 of glass is deposited using chemical vapour deposition.

Fig. 102: Pattern contacts for the seventh level mask are made using a standard contact etch for 2 micron NMOS with double level metal. This step requires spin coating of resist, exposure to the seventh mask, development of resist, ion enhanced etching, and resist stripping.

Fig. 103: A 1 micron second lev l m tal layer 517 f aluminium is vaporated ov r th wafer 500. This metal lay r 517 provides th second lev l of contacts. This is requir d because a high wiring density is required to the h at rs 514, which must be m tal for low resitance. This layer also provides th thermal diffuser or th rmal shunt as d scribed in th earlier mbodim nts.

Fig. 104: Th second l v l metal 517 is etched using an ighth mask. This step requir s spin coating of

resist, exposure to the eighth mask, d v lopment of the r sist, plasma etching, and r sist stripping. This is a normal NMOS step. The isolated metal disk above the heaters 514 is the thermal diffuser used to distribut wast heat to avoid hot-spots.

Fig. 105: A thick lay r 518 of glass is deposited over the wafer 500. The lay r 518 must be thick enough to provide adequate mechanical strength to resist the shock of imploding bubbles. Also, enough glass must be deposited to diffuse the heat over wide enough area so that the ink does not boil when in contact with it. 4 micron thickness is considered adequate, but can be easily varied if desired.

Fig. 106: This step requires etching using a ninth level mask of a cylindrical barrel 519 into the overcoat 518, through the thermal oxide layer 504 down to the implanted field 503. Both CVD glass and thermal quartz are etched. This step requires spin coating of resist, exposure to a ninth level mask, development of resist, and anisotropic ion enhanced etching, and resist stripping.

Fig. 107: The thermal chamber 520 is formed by an isotropic plasma etch of silicon, highly selective over SiO_2. This is essential, as otherwise the protective layer or SiO_2 separating the heater 514 from the passivation will be etched. The previously etched barrel 519 acts as the mask for this step. In this case, an isotropic etch of 17 microns is used. Care must be taken not to fully etch the thermal SiO_2 layer 501.

Fig. 108: Nozzle channels 521 are etched from the reverse side of the wafer 500 by an anisotropic ion enhanced etching. The channels 521 are about 60 microns in diameter, and about 500 microns deep. The depth of the channels 521 is such that the distance between the top of the channel and the bottom of the thermal chamber 520 is the required nozzle length. The etching place through a layer of resist 522.

Fig. 109: The nozzle via is etched from the front side of the wafer 500 using a highly an anisotropic ion enhanced etching. This etch is from the bottom of the the thermal chamber 520 to the top of the back etched nozzle channels 521, and is about 20 microns in length, and 20 microns in diameter. The nozzle barrels 523 are formed therefrom.

Fig. 110: A 0.5 micron passivation layer 524 of tantalum is conformably coated over the entire wafer 500.

Fig. 111: In this step, windows are opened for the bonding pads 525. This requires a resist, coating, exposure to a twelfth level mask, resist. development, etching of the tantalum passivation layer 524, ion enhance etching of the overcoat 518, and resist stripping. As 2 microns of aluminium is available in the pad regions, it is easy to avoid etching through the pads formed by the second level metal 517.

Fig. 112: After probing of the wafer 500, the ZBJ chip is mounted into a frame or support extrusion as earlier described and glued into place. Wires 526 are bonded to the pads formed by the second level metal 525 at the ends of the chip. Power rails are bonded along the two long edges of the chip. Connections are then potted in epoxy resin.

Fig. 113: This shows a forward ejection type ZBJ nozzle filled with ink 527. In this case, the droplet is ejected downwards when the nozzle fires. This type of head requires priming of ink using positive pressure, as it will not be filled by capiliary action. A similar head construction can be used for reverse firing nozzles by filling the head heat chip from the other side.

Whilst the foregoing represents a fabrication process for a general, preferred nozzle structure, similar steps, although with some differences, can be used for the specific nozzle structures illustrated in Figs. 17 to 22. Each of the following processes is a 2 micron NMOS with two level metal process as this is the simplest process which can be used to produce high resolution, high performance colour ZBJ devices. Also, the consistency between the processes permits an easier comparison therebetween.

A summary of the process steps required to provide the structure shown in Fig. 17 is as follows:

1) starting wafer: p type, 600 microns thick;
2) grow 0.15 microns silicon nitride;
3) pattern nitride using mask 1;
4) implant field;
5) grow 0.8 micron field oxide;
6) implant depletion arsenic using mask 2;
7) grow 0.1 micron gate oxide;
8) deposit polysilicon (1 micron);
9) pattern polysilicon using mask 3;
10) etch diffusion windows;
11) diffus n+ regions;
12) d posit 1 micron CVD glass;
13) pattern contacts using mask 4;
14) d posit 0.05 micron hafnium borid heater;
15) tch heat r using mask 5;

16) deposit first metal (1 micron);
17) patt rn m tal using mask 6;
18) deposit 1 micron CVD glass;
19) pattern contacts using mask 7;
20) deposit second metal (including thermal shunt), 1 micron aluminium;
21) pattern metal using mask 8;
22) deposit 10 microns CVD glass;
23) etch nozzle through CVD glass using mask 9;
24) etch thermal chamber using isotropic etch;
25) back-etch barrels through the wafer using mask 10;
26) join thermal chambers to barrels using an anisotropic, unmasked etch;
27) deposit 0.5 micron tantalum passivation;
28) open pads using mask 11;
29) wafer probe;
30) mount into head assembly;
31) bond wires;
32) pot in epoxy;
33) fill with ink. Head will fill by capillarity.

A summary of the process steps required to provide the structure shown in Fig. 18 is as follows:

1) starting wafer: p type, 600 microns thick;
2) grow 0.15 microns silicon nitride
3) pattern nitride using mask 1;
4) implant field;
5) grow 0.8 micron field oxide;
6) implant depletion arsenic using mask 2;
7) grow 0.1 micron gate oxide;
8) deposit polysilicon (1 micron);
9) pattern polysilicon using mask 3;
10) etch diffusion windows;
11) diffuse n+ regions;
12) deposit 1 micron CVD glass;
13) pattern contacts using mask 4;
14) deposit 0.05 micron HfB_2 heater;
15) etch heater using mask 5;
16) deposit first metal (1 micron);
17) pattern metal using mask 6;
18) deposit 1 micron CVD glass;
19) pattern contacts using mask 7;
20) deposit second metal (including thermal diffuser), 1 micron aluminium;
21) pattern metal using mask 8;
22) deposit 3 microns CVD glass;
23) etch entrance to thermal chamber through CVD glass using mask 9;
24) etch thermal chamber using isotropic plasma etch;
25) etch holes 520 microns deep, 80 microns wide from the back side of the wafer, using mask 10;
26) join thermal chambers to barrels using an anisotropic RIE using thermal chamber entrance as a mask;
27) deposit 0.5 micron tantalum passivation;
28) open pads using mask 11;
29) wafer probe;
30) bond wires;
31) pot in epoxy
32) mount into head assembly;
33) fill head assembly with ink;
34) prim head with positiv ink pressur above the bubbl pr ssur of th nozzl .

A summary of th process st ps required to provid th structur shown in Fig. 19 is as follows:

1) starting waf r: p type, 600 microns thick;
2) grow 0.15 microns silicon nitrid ;
3) pattern nitrid using mask 1;

4) implant fi ld;
5) etch a circular tr nch around th nozzle position. 22 microns diameter, 2 microns deep, 1 micron wid using mask 2;
6) grow 0.4 micron fi ld oxid (this also grows on th tr nch walls);
7) deposit 0.05 micron HfB_2 heater;
8) etch heater using mask 3;
9) implant arsenic using mask 4;
10) grow 0.1 micron gate oxide;
11) deposit polysilicon (1 micron);
12) pattern polysilicon using mask 5;
13) etch diffusion windows;
14) diffuse n+ regions;
15) deposit 1 micron CVD glass;
16) pattern contacts using mask 6;
17) deposit first metal (1 micron);
18) pattern metal using mask 7;
19) deposit 1 micron CVD glass;
20) pattern contacts using mask 8;
21) deposit second metal, 1 micron aluminium;
22) pattern metal using mask 9;
23) deposit 20 microns CVD glass, forming the nozzle layer;
24) anisotropically etch thermal chamber and nozzle using mask 10 (undersized diameter of less than 18 microns);
25) etch holes 520 microns deep, 80 microns wide from the back side of the wafer, using mask 11. Join to nozzles.
26) use a silicon specific isotropic "wash" etch to enlarge the thermal chamber to the edge of to the heater trench;
27) deposit 0.5 micron tantalum passivation;
28) open pads using mask 12;
29) wafer probe;
30) bond wires;
31) pot in epoxy;
32) mount into head assembly;
33) fill head assembly with ink.

A summary of the process steps required to provide the structure shown in Fig. 20 is as follows:
1) starting wafer: p type, 600 microns thick;
2) grow 0.15 microns silicon nitride;
3) pattern nitride using mask 1;
4) implant field;
5) etch a circular trench around the nozzle position. 22 microns diameter, 2 microns deep, 1 micron wide using mask 2;
6) grow 0.4 micron field oxide (this also grows on the trench walls);
7) deposit 0.05 micron HfB_2 heater;
8) etch heater using mask 3;
9) implant arsenic using mask 4;
10) grow 0.1 micron gate oxide;
11) deposit polysilicon (1 micron);
12) pattern polysilicon using mask 5;
13) etch diffusion windows;
14) diffuse n+ regions;
15) deposit 1 micron CVD glass;
16) pattern contacts using mask 6;
17) deposit first metal (1 micron);
18) patt rn m tal using mask 7;
19) d posit 1 micron CVD glass;
20) patt rn contacts using mask 8;
21) d posit second m tal (including th rmal diffuser), 1 micron aluminium;
22) patt rn m tal using mask 9;

23) deposit 3 microns CVD glass;
24) anisotropically etch th rmal chamber and nozzle using mask 10 (und rsized diam ter of less than 18 microns to avoid tching heat rs);
25) tch holes 520 microns d p, 80 microns wid from th back side of th waf r, using mask 11. Join to nozzles.
26) use a silicon specific isotropic "wash" etch to enlarge the thermal chamber to the edge of to the heater trench;
27) deposit 0.5 micron tantalum passivation;
28) open pads using mask 12;
29) wafer probe;
30) bond wires;
31) pot in epoxy;
32) mount into head assembly;
33) fill head assembly with ink.

A summary of the process steps required to provide the structure shown in Fig. 21 is as follows:
1) starting wafer: p type, 600 microns thick;
2) grow 0.15 microns silicon nitride;
3) pattern nitride using mask 1;
4) implant field;
5) grow 0.7 micron field oxide;
6) implant arsenic using mask 2;
7) grown 0.1 micron gate oxide;
8) deposit polysilicon (1 micron);
9) pattern polysilicon using mask 3;
10) etch diffusion windows;
11) diffuse n+ regions;
12) etch a 2 micron deep circular depression slightly wider than the nozzle diameter using mask 4;
13) deposit 1 micron CVD glass;
14) pattern contacts using mask 5;
15) deposit 0.05 micron HfB_2 heater;
16) etch heater anisotropically (in the vertical direction only) using mask 6;
17) deposit first metal (1 micron);
18) pattern metal using mask 7;
19) deposit 1 micron CVD glass. This provides inter- level dielectric, as well as covering the heater.
20) pattern contacts using mask 8;
21) deposit second metal (including thermal diffuser), 1 micron aluminium;
22) pattern metal using mask 9;
23) deposit 20 microns CVD glass;
24) anisotropically etch nozzle into CVD glass using mask 10;
25) etch the silicon thermal chamber anisotropically using an ion assisted plasma etch specific for silicon, using CVD glass nozzle as a mask;
26) etch holes 520 microns deep, 80 microns wide from the back side of the wafer, using mask 11. Join to thermal chambers;
27) deposit 0.5 micron tantalum passivation;
28) open pads using mask 12;
29) wafer probe;
30) bond wires;
31) pot in epoxy;
32) mount into head assembly;
33) fill head assembly with ink.

A summary of the process steps required to provide the structure shown in Fig. 22 is as follows:
1) starting wafer: p type, 600 microns thick;
2) grow 0.15 microns silicon nitride;
3) patt rn nitrid using mask 1;
4) implant field;
5) grow 0.7 micron fi ld oxide;
6) implant ars nic using mask 2;
7) grown 0.1 micron gate oxid ;

8) deposit polysilicon (1 micron);
9) pattern polysilicon using mask 3;
10) tch diffusion windows;
11) diffus n+ regions;
12) etch a 2 micron deep circular depression slightly wider than the nozzle diameter using mask 4;
13) deposit 1 micron CVD glass;
14) pattern contacts using mask 5;
15) deposit 0.05 micron HfB_2 heater;
16) etch heater anisotropically (in the vertical direction only) using mask 6;
17) deposit first metal (1 micron);
18) pattern metal using mask 7;
19) deposit 1 micron CVD glass. This provides inter- level dielectric, as well as covering the heater.
20) pattern contacts using mask 8;
21) deposit second metal (including thermal diffuser), 1 micron aluminium;
22) pattern metal using mask 9;
23) deposit 3 microns CVD glass;
24) anisotropically etch thermal chamber into CVD glass using mask 10;
25) etch silicon nozzle anisotropically using an ion assisted plasma etch specific for silicon, using CVD glass hole as a mask;
26) etch holes 520 microns deep, 80 microns wide from the back side of the wafer, using mask 11. Join to nozzles;
27) deposit 0.5 micron tantalum passivation;
28) open pads using mask 12;
29) wafer probe;
30) bond wires;
31) pot in epoxy;
32) mount into head assembly;
33) fill head assembly with ink.

The ZBJ printhead 200 incorporating the ZBJ chip 100 is useful in a variety of printing applications either printing across the page in the traditional manner, as a scanning print head, or as a stationary full width print head. Figs. 114 to 118 show various configurations for use of a number of ZBJ heads.

Fig. 114 shows a colour photocopier 531 which includes a scanner 541 for scanning a page to be copied. The scanner 541 outputs red, green and blue (RGB) data to a signal processor 543 which converts the RGB data into dot screened cyan, magenta, yellow and black (CMYK) suitable for printing using the device 100. The CYMK data is input to a data formatter 545 which acts in a manner of the circuitry depicted in Figs. 56 and 57. The data formatter 545 outputs to a full colour ZBJ head 550 capable of printing at 400 pixels per inch across an A3 page carried by a paper transport mechanism 547. A controlling microcomputer 549 co-ordinates the operation of the photocopier 531 through a sequencing control of the scanning 541, signal processor 543, and paper transport mechanism 547.

Fig. 115 shows a colour facsimile machine 533 which includes some components designated in a similar manner to that of Fig. 114. The scanner 541 scans a page to be transmitted after which the scanned data of the image is compressed by a compressor 560. The compressor 560 can use any standard data compression system for images such as the JPEG standard. The compressor 560 outputs transmit data to a modem 562 which connects to a PSTN or ISDN network 564. The modem 562 receives data and outputs to an image expander 566, complementary to the compressor 560. The expander 566 outputs to the data formatter 545 in the manner described above. In this configuration a colour ZBJ head 551 of a size greater than the full width of the paper to be printed is used.

Fig. 116 shows a computer printer 535 which can print either colour or black and white images depending on the type of ZBJ head used. Data is supplied via an input 569 to a data communications receiver 568. A microcontroller 549 buffers received data to an image memory 571 which outputs to a full colour data formatter in the manner described above or a simple black and white data formatter. In this embodiment the data formatter 545 outputs to a full length ZBJ head 552 for printing on paper carried by the paper transport mechanism 547.

In Fig. 117 a video print r 537 is shown which acc pts video data via an input 574 which is input to a tel vision decoder and ADC unit 573 which outputs image pixel data to a fram stor 575. A signal processor 543 converts RGB data to CMYK data for printing in th mann r previously described. A small colour ZBJ head 553 prints n a photographed sized paper carried by th paper transport 547 for printing.

Finally Fig. 118 shows th configuration of a simpl printer 539 in which pag formatting is perform d in

a host computer 577. Th comput r 577 outputs data and control information to a buff r 579 which outputs to the data formatter 545 in th manner described above. A simpl control logic unit 581 also receives commands from th host comput r 577 for control of th paper transport mechanism 547.

Furthermore, thos skilled in th art will r alis that any combination of ZBJ h ads can be used in any of the above embodiments. For example, multi-head redundancy as previously described can be used in both page printing and scanning heads. For ultra-high resolution (1600 dpi) monochrome printing can be used in any embodiment.

The foregoing only describes a number of embodiments of the present invention and modifications, obvious to those skilled in the art can be made thereto without departing from the scope of the present invention.

TABLE 1

Application/ Feature	1.Scanning Contone colour ZBJ Head	2.Scanning Grey Tone ZBJ Head	3.Photo Size Contone Color ZBJ Head	4.Full Width A1 Contone Color ZBJ Head
Chip Size (mm)	10 X 4	10 X 1.5	100 X 2	220 X 4
No. of Nozzles	2048	512	5120	51200
No. of Pixels	128	128	1280	3200
Nozzles Per Pixel Per Color	4	4	1	4
No. of colours	4	1	4	4
Print Speed	3 mins (A4)	3 mins (A4)	8 sec (photo)	3.7 sec (A4)
Tone	FULL	GREY	SCALE	
Resolution (pixel/inch)	400	400	400	400

... continued

TABLE 1

Application/ Feature	5.Full Width A4 Bilevel ZBJ Head	6.High Specd A3 Contone colour ZBJ Head	7.Medium Speed A3 Contone colour ZBJ Head
Chip Size (mm)	220 × 2	310 × 4	310 × 2
No. of Nozzles	12800	71680	17920
No. of Pixels	12800	4480	4480
Nozzles Per Pixel Per Color	1	4	1
No. of colours	1	4	4
Print Speed	3.7 sec (A4)	5.3 sec (A3)	21 sec (A3)
Tone	FULL	GREY	SCALE
Resolution (pixel per inch)	1600	400	400

TABLE 2

Fault	Consequence
Main drive track open	Main heater fails, redundant heater takes over.
Redundant drive track open	Redundant heater fails: no effect.
V+ track open	Block of 32 heaters fail, redundant heaters take over.
Ground open	Block of 32 redundant heaters fail: no effect.
Two main drive tracks shorted	Both nozzles will fire.
Two redundant drive tracks shorted	No effect.
Main drive track shorted to redundant drive tack	Both heaters will be in series between V+ and ground, and constantly on at half power. Either the main heater or the redundant heater will overheat and go open circuit (under normal conditions, average power is 1/32 of pulse power). The other heater will take over.
Main drive track shorted to V+	Drive transistor will fuse when turned on. Redundant circuit takes over.
Main drive track shorted to ground	Main heater will overheat as it is constantly on. It will go open circuit. The redundant circuit will take over.

... continued

TABLE 2

Redundant drive track shorted to V+	Redundant heater will overheat as it is constantly on. It will go open circuit. No effect.
Redundant drive track shorted to ground	Redundant transistor will fuse if ever turned on. No effect if main circuit works.
V+ shorted to ground	short, V+ track or Ground track will fuse. If V+ track fuses, redundant circuits will take over from isolated main circuits. Other conditions have no effect.
Sense track open	Redundant circuit will not operate: no effect.
Other conditions of sense track	Same as for main drive

The present invention had been described in detail with respect to preferred embodiments, and it will now be apparent from the foregoing to those skilled in the art that changes and modifications may be made without departing from the invention in its broader aspects, and it is the intention, therefore, in the appended claims to cover all such changes and modifications as fall within the true spirit of the invention.

A bubblejet print device (100) is disclosed which is integrally formed having arrays (102,103,104,105) of nozzles (110) which form part of a passageway communicating between opposite surfaces of a semiconductor substrate (130). Each nozzle (110) has an integrally formed heater (120) which permits heating of ink (106) within the respective nozzle (110) for the ejection of an ink drop (108) therefrom. The heater (120) can provide a fault tolerant structure through the provision of a main heater (121,441) and a redundant heater (122,443) each of which can be separately energised from a corresponding electronic drive circuit (160, 165). Several methods of manufacturing the device (100) using semiconductor fabrication techniques are also disclosed. A bubblejet print head (200) incorporating the device (100) can form part of an image reproducing apparatus (531,533,535,537) and is capable of printing full colour images at 400 dpi and monochrome images up to 1600 dpi. An ink drop size of about 3 picolitres is used for these image intensities. A thermal shunt (140) or diffuser (491) are used to transport heat away from the heater (120) to prevent formation of hot spots thereabout after the ejection of an ink drop (108). Electronic circuitry (310,302-305) is disclosed which is used to couple data to the device (100) to provide full width page printing using a stationary head (200) and a moving paper medium (220).

Claims

1. A bubblejet print device characterized by comprising a plurality of nozzles each communicating with a corespondent passageway for the supply of ink to the nozzle, and a plurality of heater means each of which is associated with a corresponding nozzl or passageway, characterised in that said heat r m ans comprises a plurality of heat rs each of which has a corr sponding electronic drive circuit.

2. A d vic as claimed in claim 1, charact rised in that said h at r m ans surrounds th corresponding nozzl or passag way.

3. A device as claimed in claim 2, characterised in that said heater means is substantially annular.

4. A device as claimed in claim 1, 2 or 3, characterised in that said heat r means comprises two heat rs.

5. A device as claimed in claim 4, characterised in that each said heater is serpentine within a semi-circular configuration.

6. A device as claimed in claim 4, characterised in that each said heater is a flat spiral having a part-turn or turns interleaved with the other heater.

7. A device as claimed in claim 4, characterised in that the electronic drive circuit of one of said heaters is connected with the drive circuit of the other heater and operable only in the event that said other heater fails to operate.

8. A device as claimed in claim 7, characterised in that said device is fabricated on a semiconductor substrate and the two drive circuits are fabricated on said substrate at locations which are not adjacent.

9. A device as claimed in claim 8, characterised in that said heater means is located between said two drive circuits.

10. A device as claimed in claim 7, characterised in that each said drive circuit contains a heater switching semiconductor switch, said switches are of a like polarity type, and the connection between said one drive circuit and the other drive circuit includes voltage level shifting means connected to the switching input of said semiconductor switch of said one drive circuit.

11. A bubblejet print device characterised by comprising a plurality of nozzles each communicating with a corresponding passageway for the supply of ink to the nozzle and a plurality of heater means each of which is associated with a corresponding nozzle or passageway, characterized in that each said heater means has a plurality of electronic drive circuits, said heater means and the corresponding electronic drive circuits being integrally formed on a substrate and spaced apart in relation to each other.

12. A device as claimed in claim 11, characterised in that each said heater means comprises two heaters each with a corresponding said electronic drive circuit, said heater means being located between said drive circuits.

13. A device as claimed in claim 12, characterised in that said drive circuits are arranged adjacent the periphery of the substrate.

14. A bubblejet print device characterised by comprising a first plurality and a second plurality of nozzles each communicating with a corresponding passageway for the supply of ink to the nozzle, and a first plurality and a second plurality of heater means each associated with a corresponding one of said nozzles or passageways, characterised in that for each of said first plurality of nozzles and heater means there is a corresponding one of said second plurality of nozzles and heater means allocated thereto, and each heater means of said second plurality of nozzles is interconnected to the allocated one of said first pluralily of said heater means to sense the failure thereof and be enabled thereby.

15. A device as claimed in claim 14, characterised in that the interconnection of said second plurality of said heater means include compensation means adapted to compensate for any spacial separation of said second plurality of nozzles from said first plurality of nozzles.

16. A device as claimed in claim 14 or 15, characterised in that each of said first plurality of said heater means comprises two independently energizable heaters and each of said second plurality of heater means is energizable after failure of both said heaters of the corresponding one of said first plurality of heat r means.

17. A bubblej t printing assembly charact rised by comprising a plurality of bubblejet printing d vic s each comprising a plurality of nozzles each communicating with a corr sponding passag way for th supply of ink to th nozzl and heat r means associated with each said nozzl or passageway, charact rised

in that for each intended print location of said assembly one or more nozzles of each said device is allocated thereto, and sensing means interconnect each nozzle of one of said devices with its corresponding allocated nozzle on another of said devices to sense the failure of the heater means, of that nozzle and enable operation of the heater means of the allocated nozzle of said another said device.

18. An assembly as claimed in claim 17, further characterised by comprising compensating means associated with each said sensing means for compensation for any spacial separation between said devices thereby permitting printing by said allocated nozzles of said another device at the print locations of the corresponding nozzles of said one device.

FIG.1
(PRIOR ART)

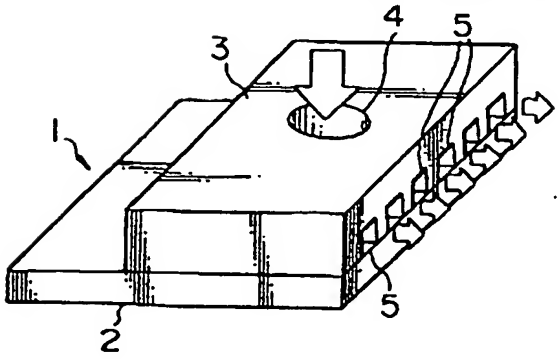


FIG.2
(PRIOR ART)

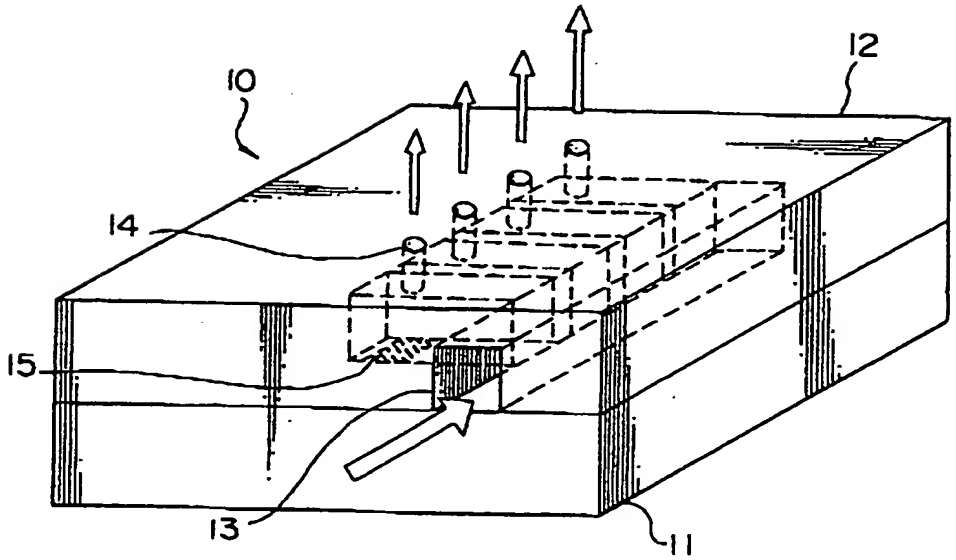


FIG. 3

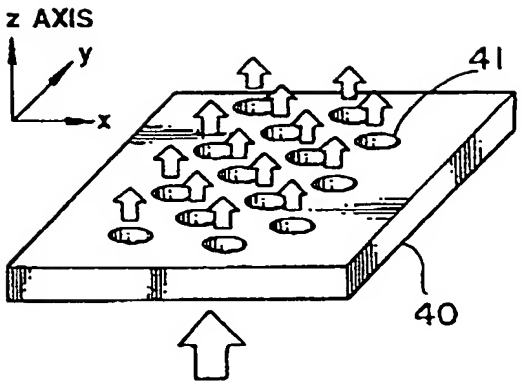


FIG. 4

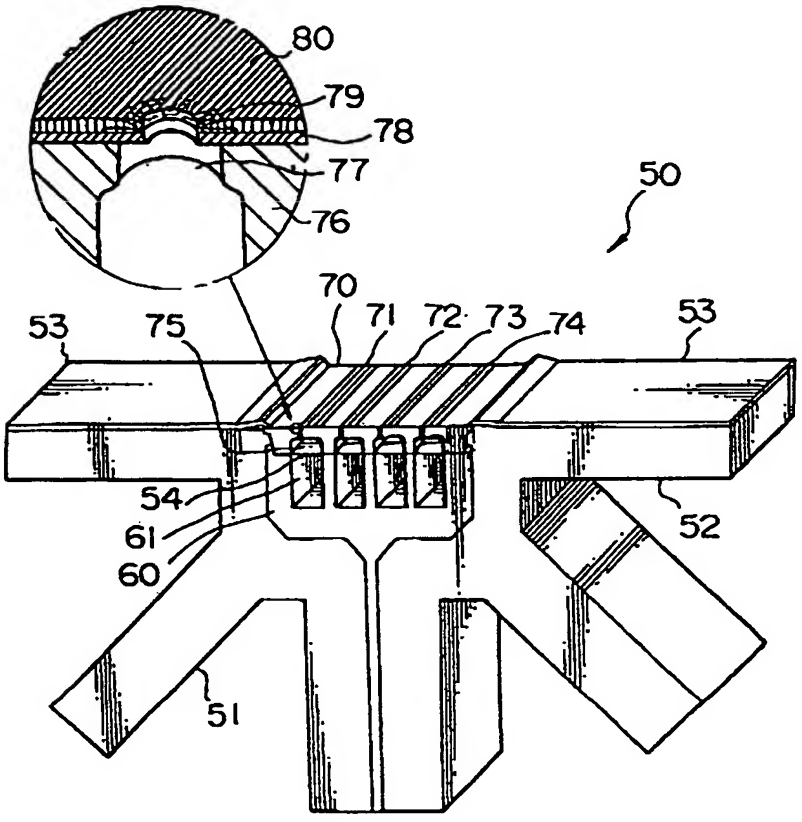
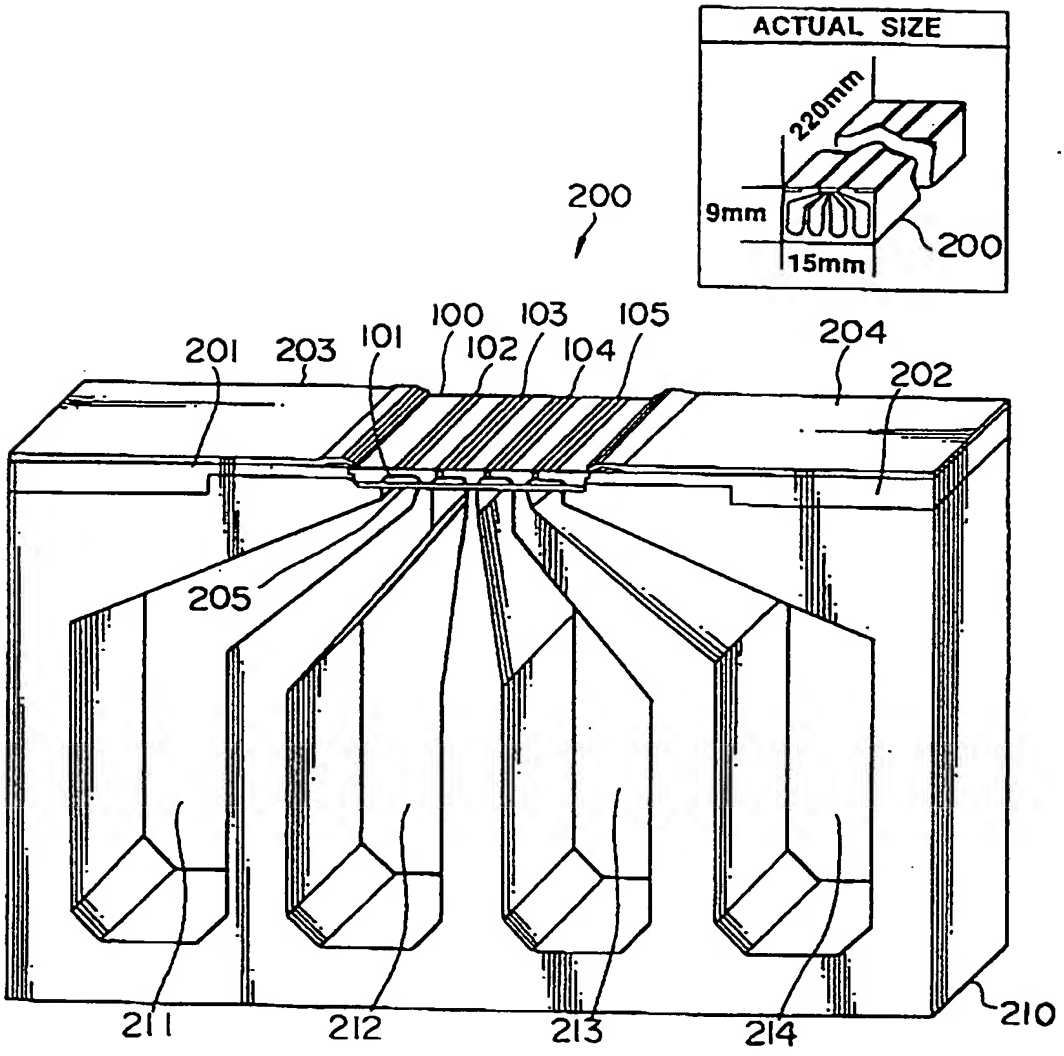


FIG. 5


ACTUAL SIZE
220mm
9mm
15mm
200
200
201
203
101
100
102
103
104
105
204
202
205
211
212
213
214
210

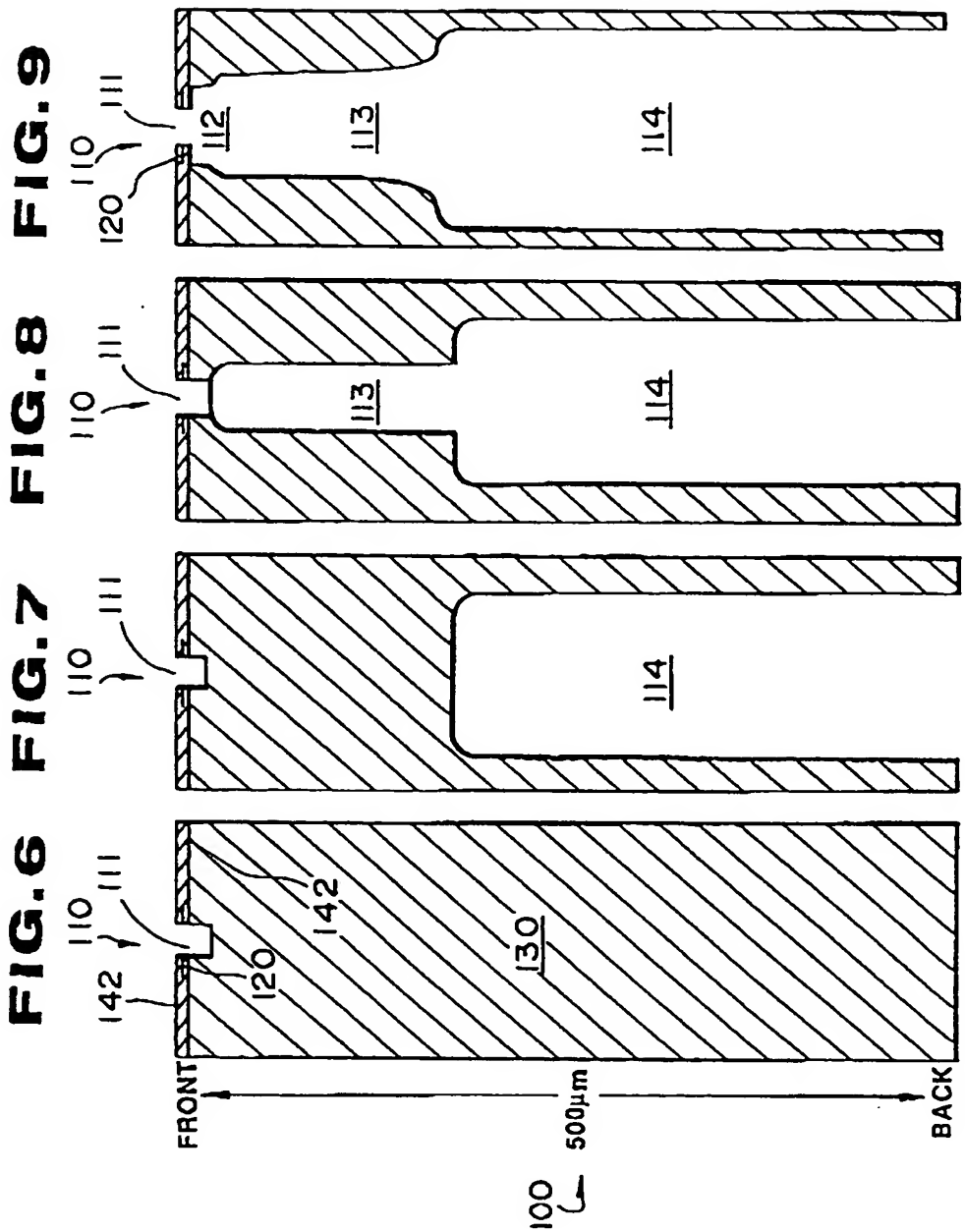


FIG.6
FIG.7
FIG.8
FIG.9
110
111
142
120
130
113
114
112
FRONT
500μm
BACK
100

FIG.10

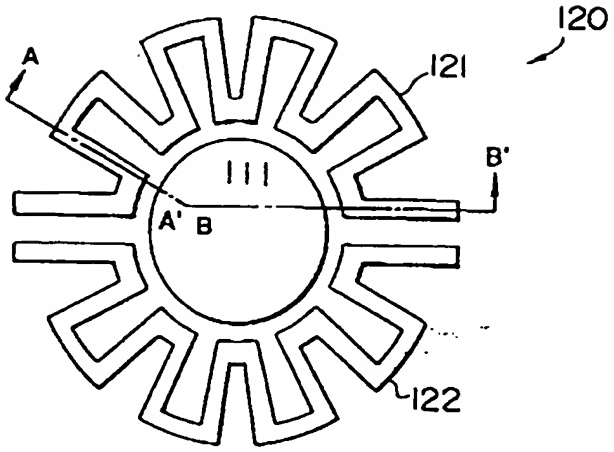


FIG.11

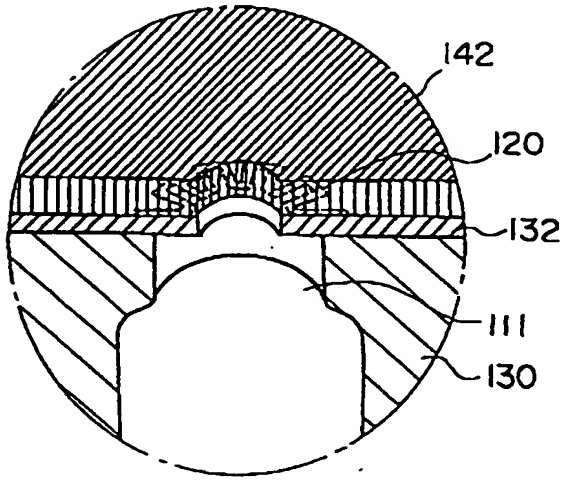


FIG.12

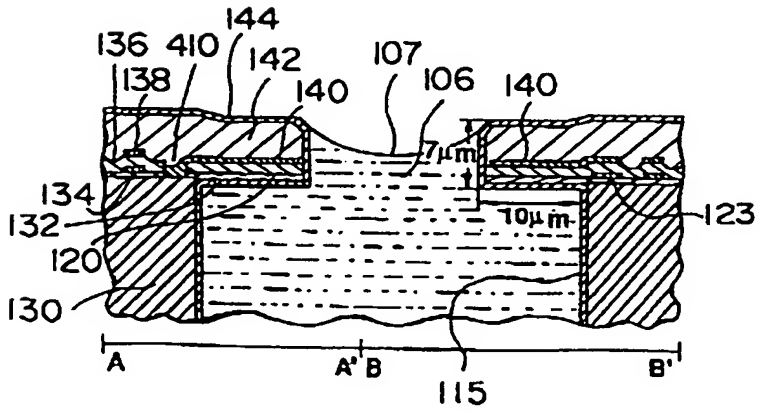


FIG.13

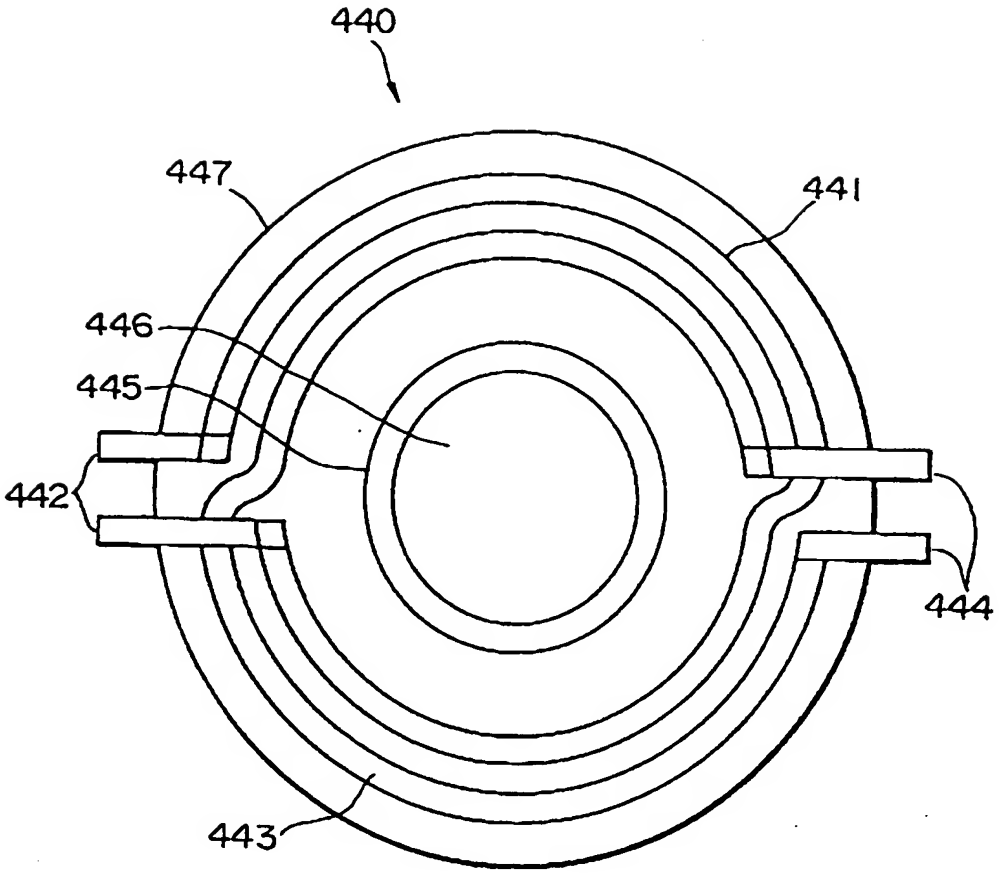


FIG.14

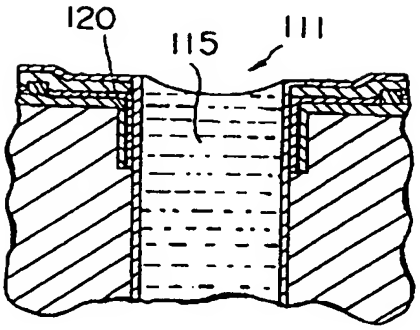


FIG.15

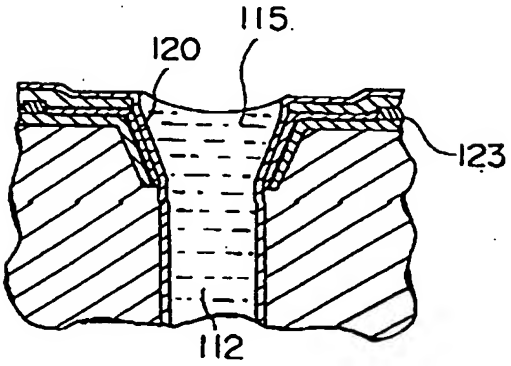


FIG.16

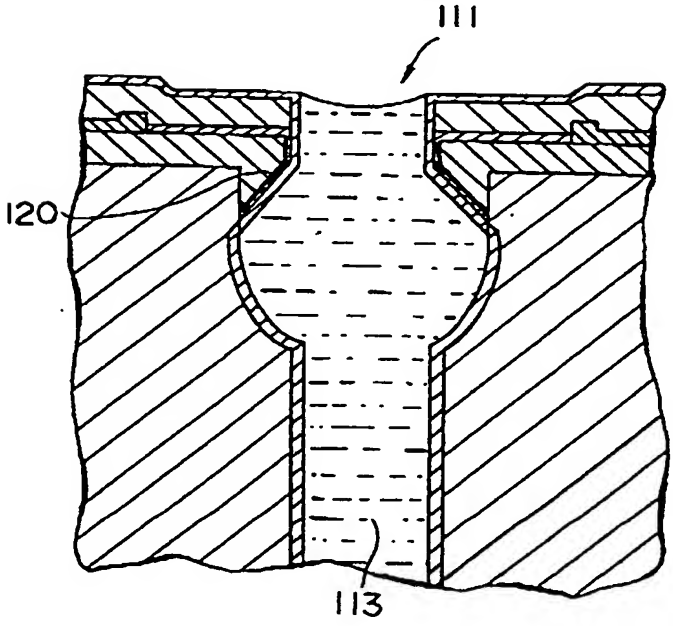


FIG.17

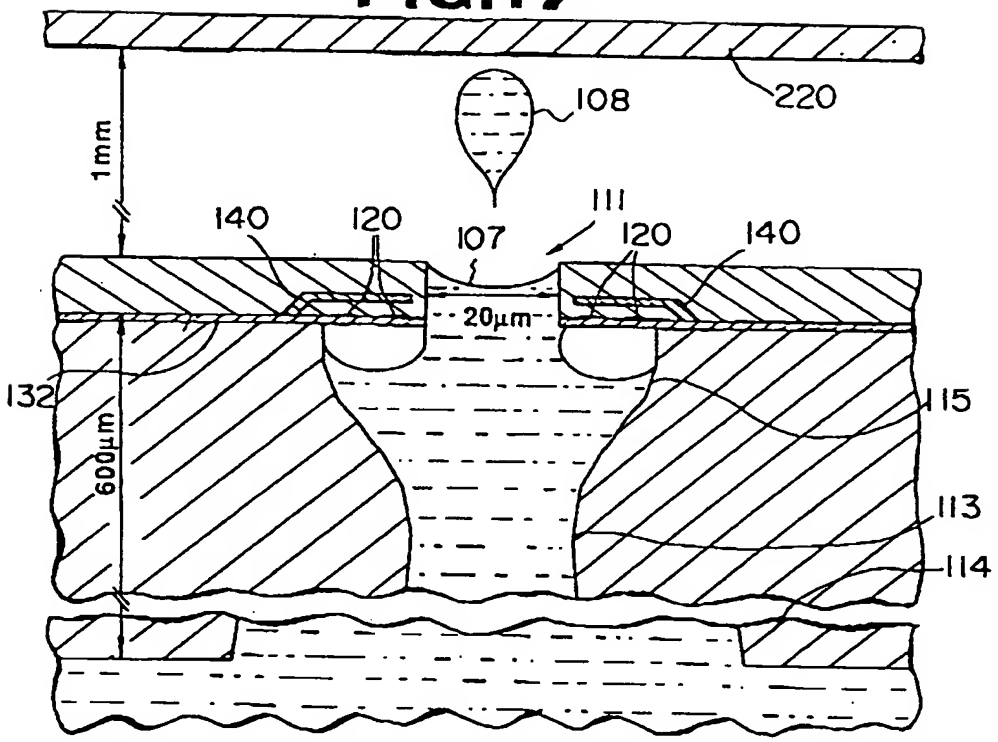

220
108
1mm
140
120
107
111
120
140
20μm
132
600μm
115
113
114

FIG.18

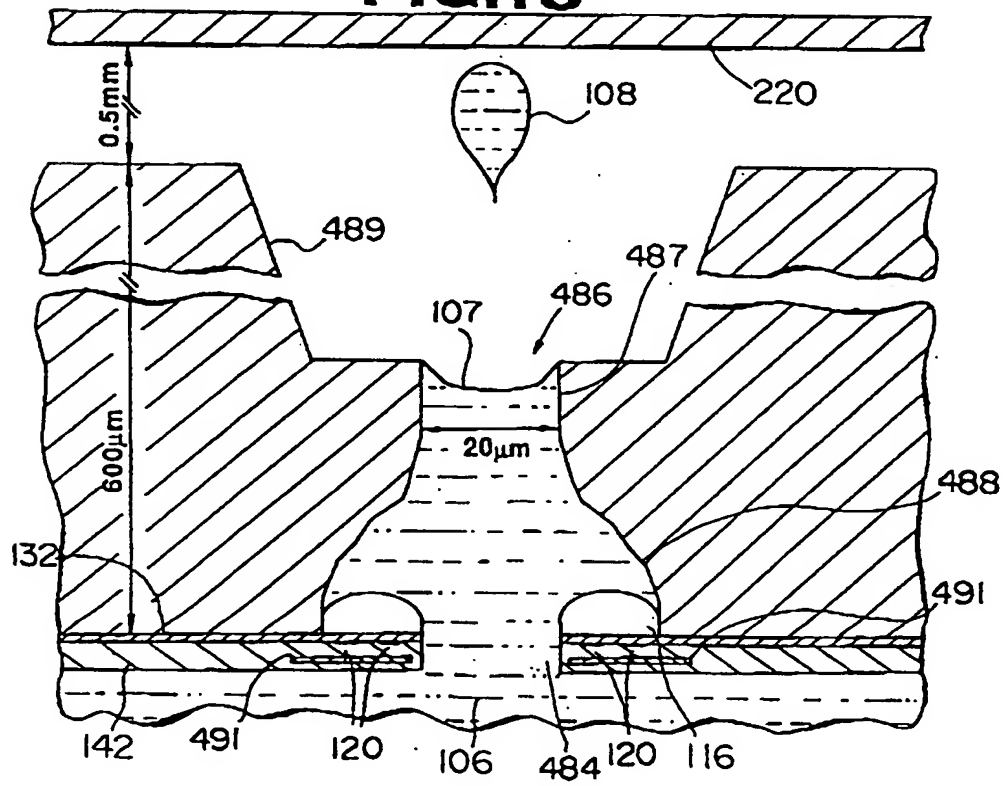

220
108
0.5mm
489
487
107
486
20μm
600μm
488
132
491
142
491
120
106
484
120
116

FIG.19

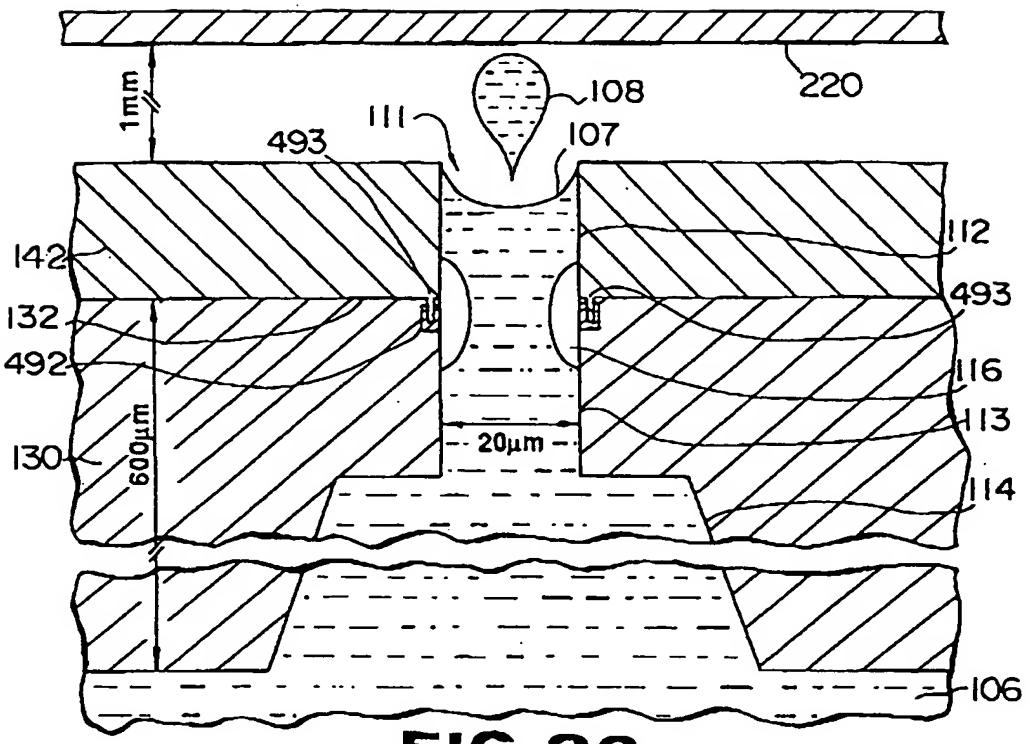

220
1mm
108
111
107
493
112
142
493
132
492
116
113
600µm
20µm
130
114
106

FIG.20

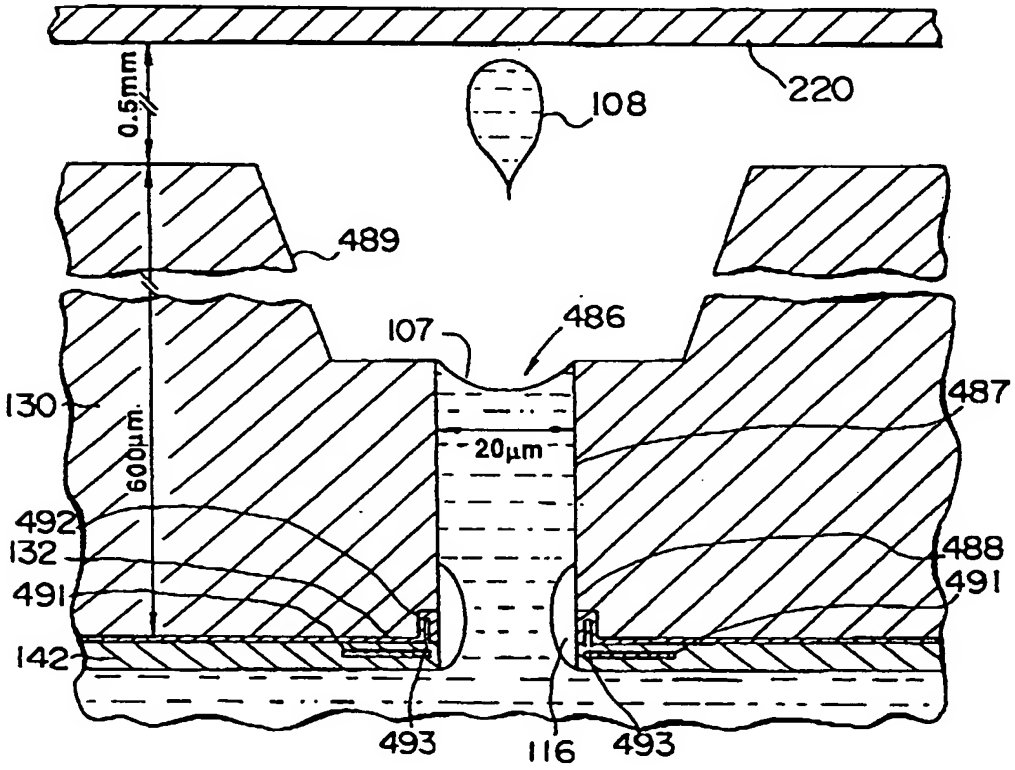

220
0.5mm
108
489
107
486
487
130
600µm
20µm
492
132
488
491
491
142
493
116
493

FIG.21

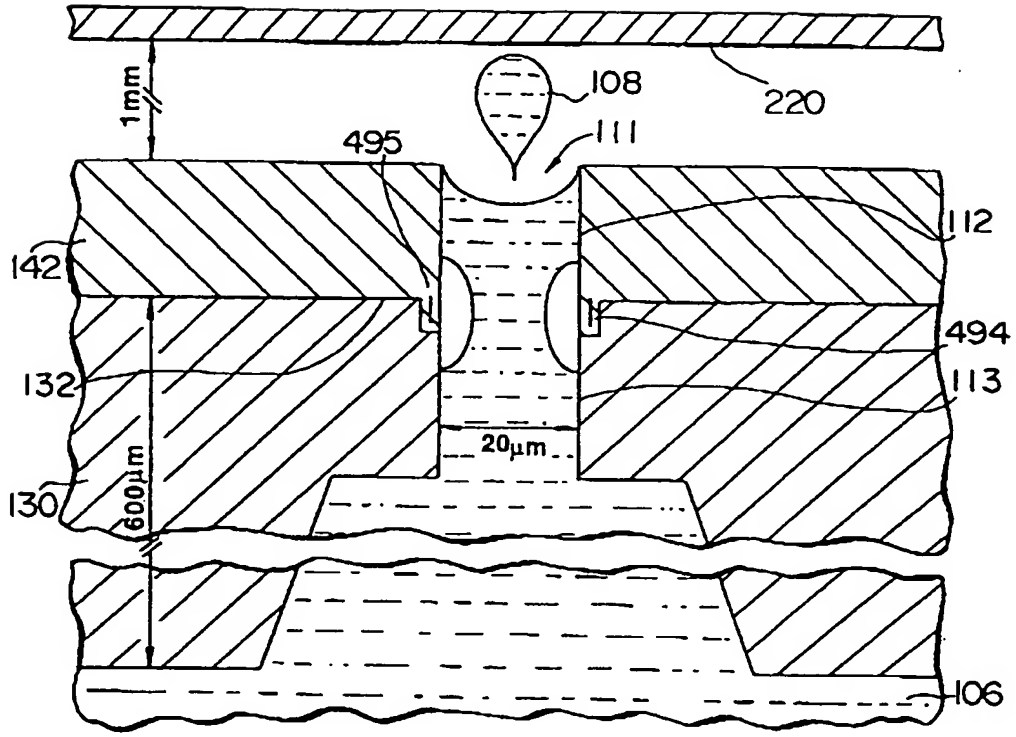

1mm
108
220
111
495
112
142
494
132
113
20µm
600µm
130
106

FIG.22

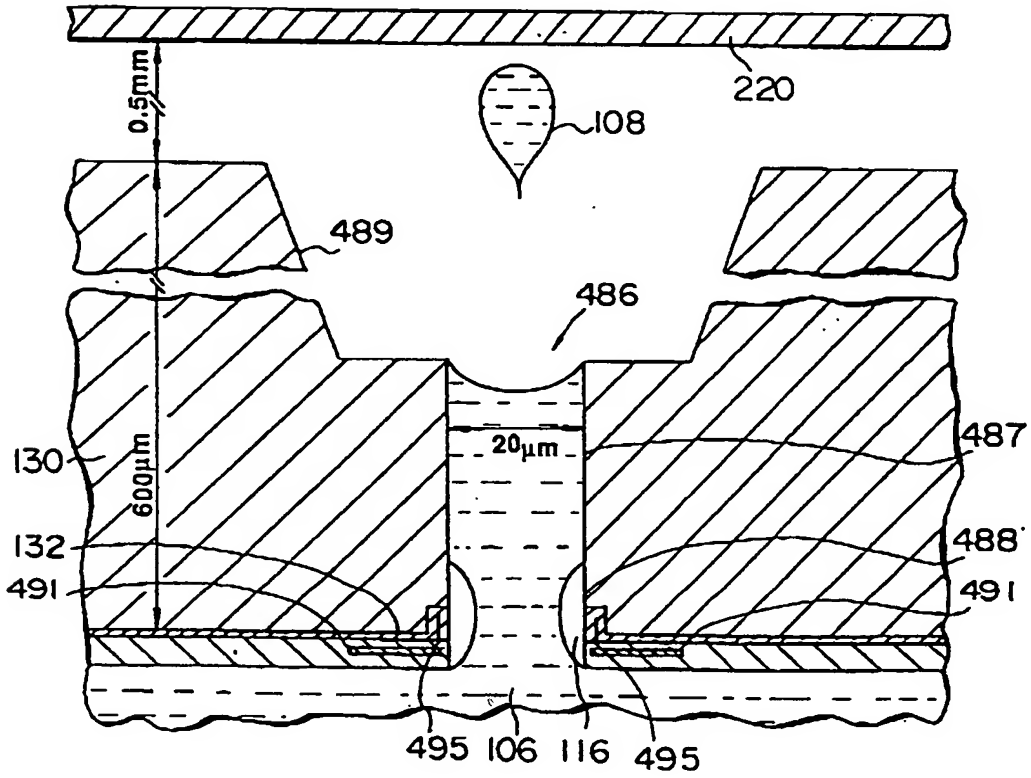

0.5mm
220
108
489
486
20µm
487
130
600µm
132
488
491
491
495
106
116
495

FIG.23

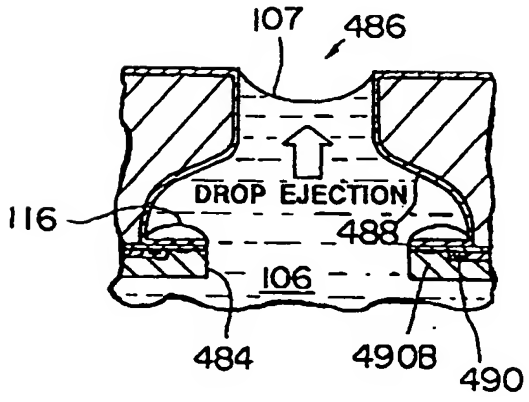


FIG.24

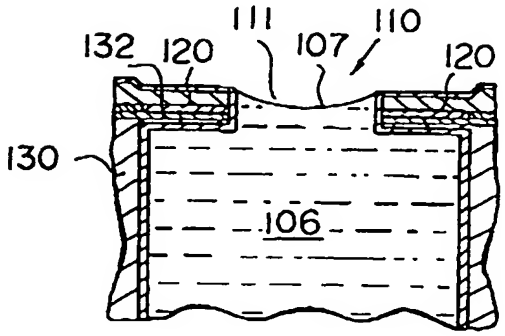


FIG.25

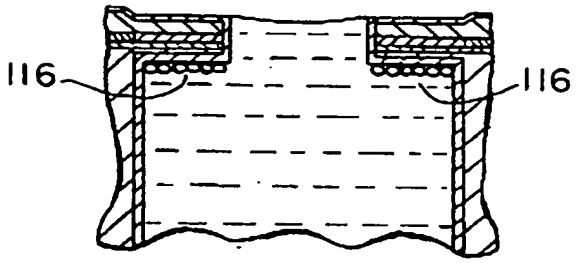


FIG.26

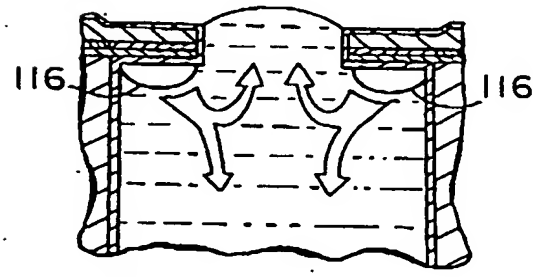


FIG.27

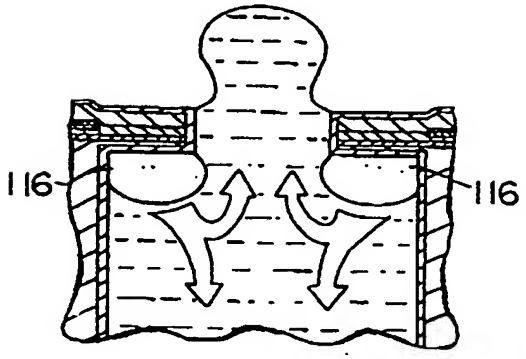


FIG.28

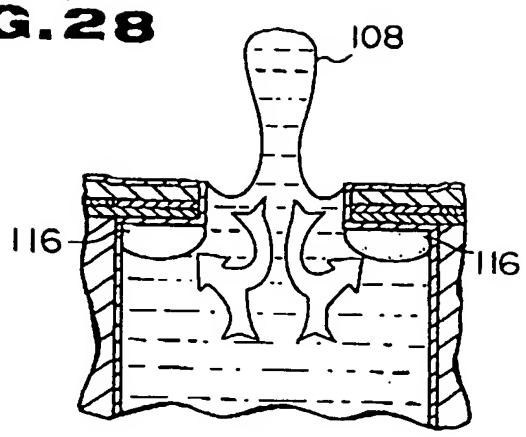


FIG.29

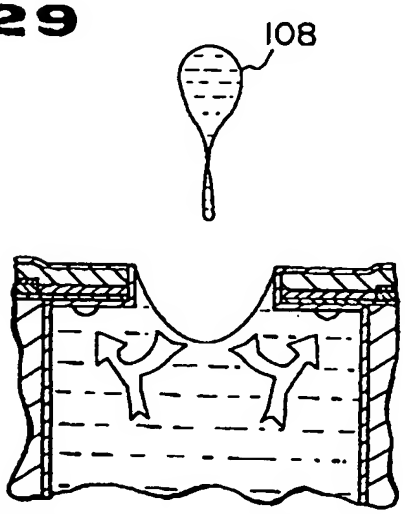


FIG.30

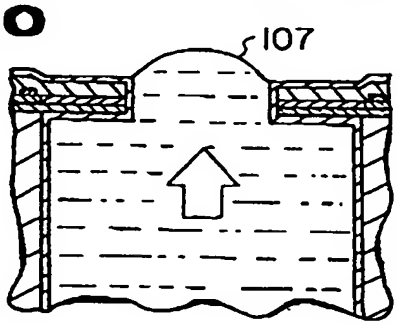


FIG.31

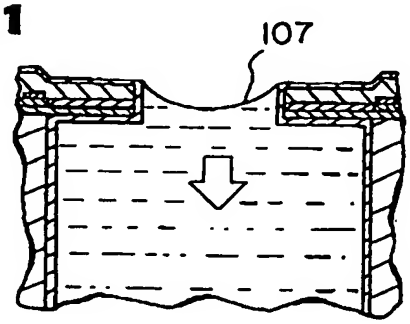


FIG.32

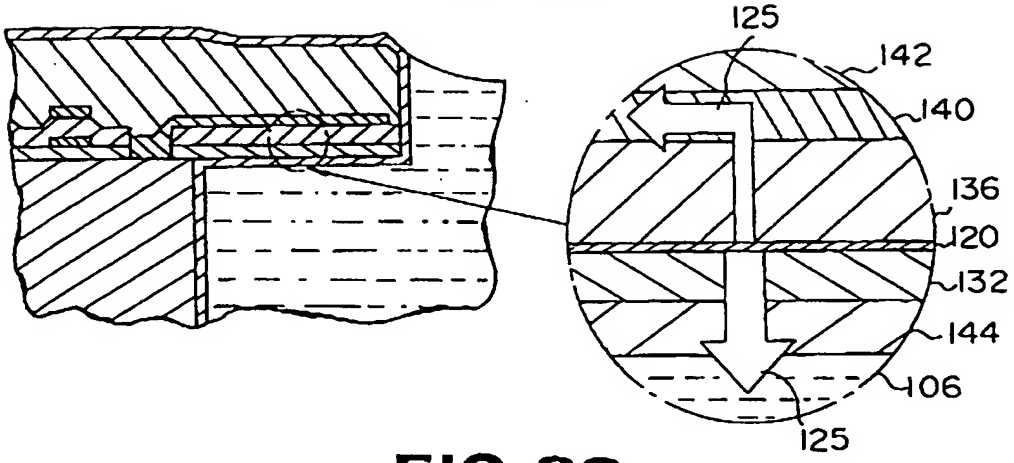


FIG.33

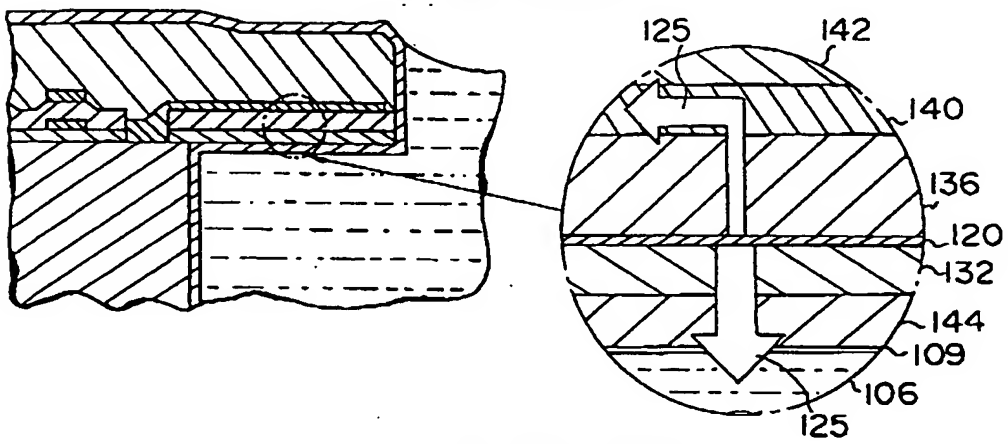


FIG.34

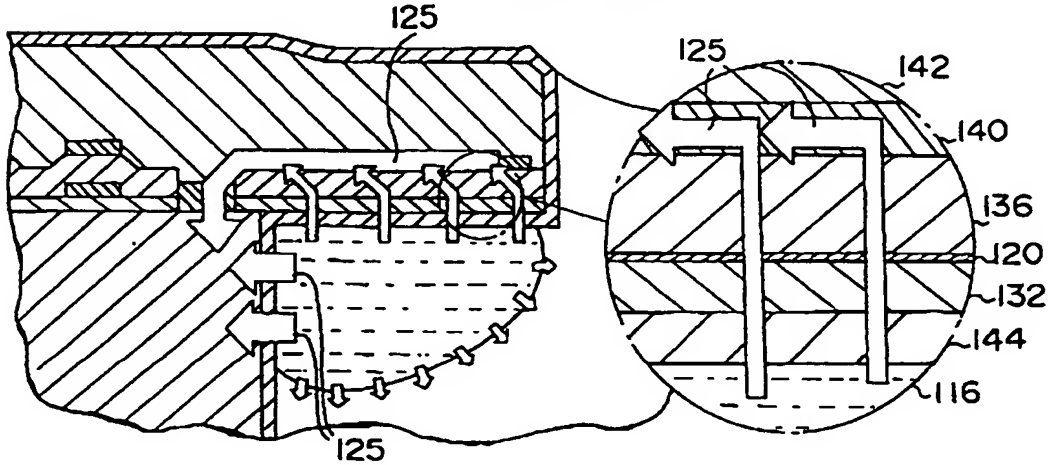


FIG. 35

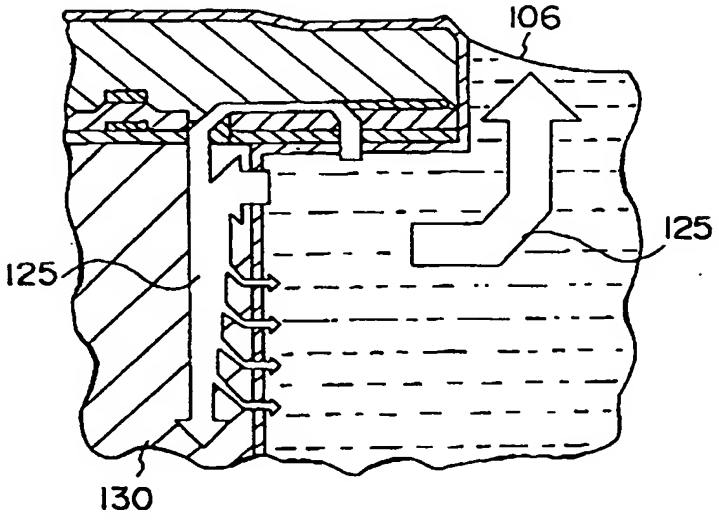


FIG. 36

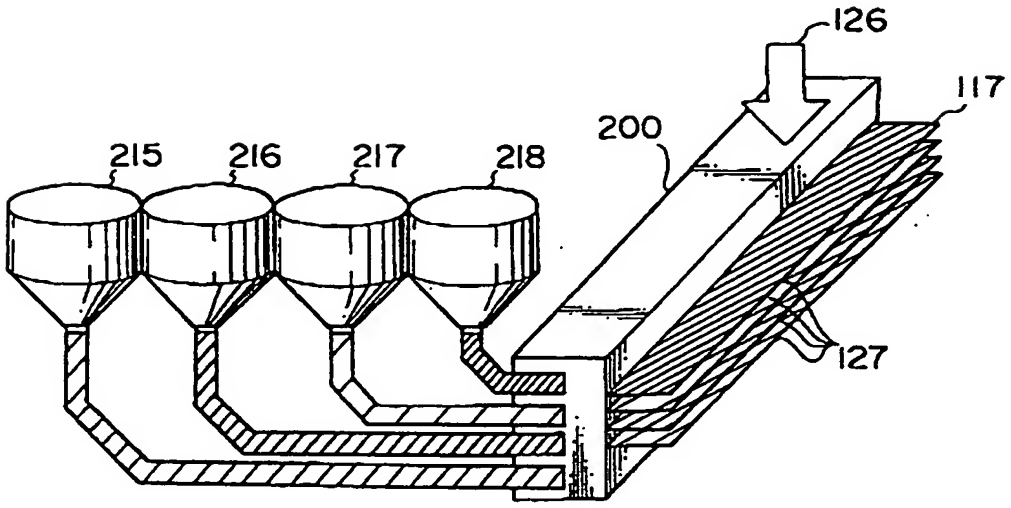


FIG. 37

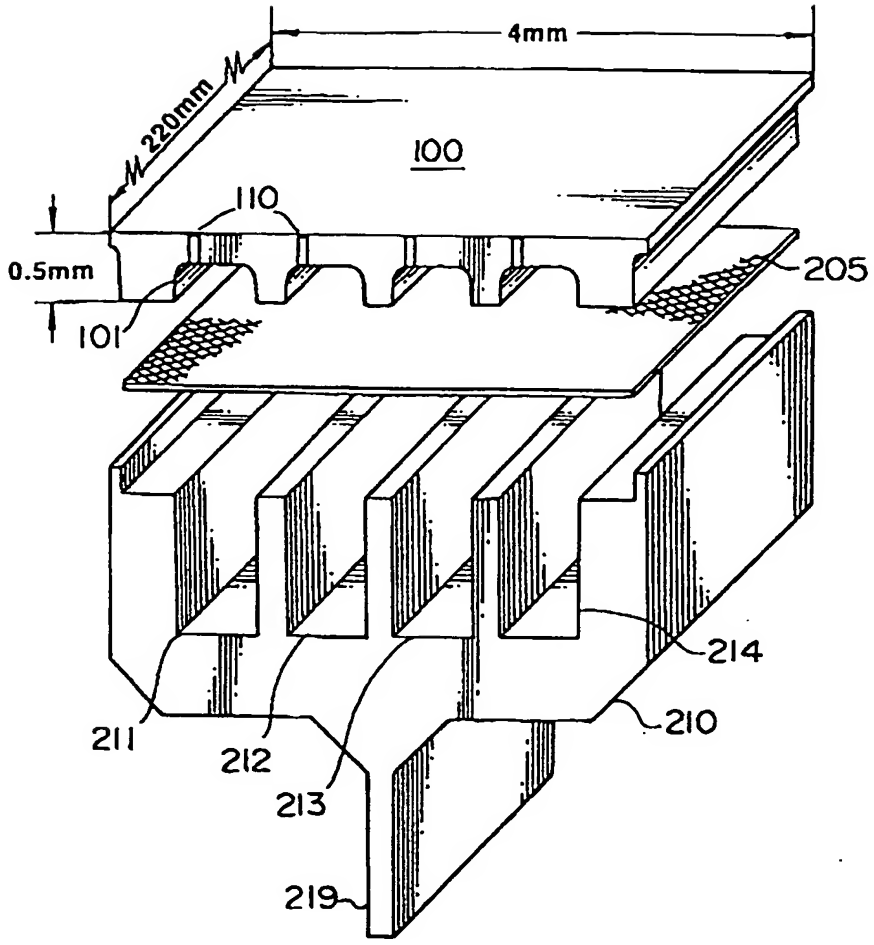

4mm
220mm
100
110
0.5mm
101
205
214
210
211
212
213
219

FIG. 38

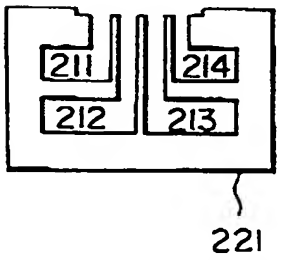

211
214
212
213
221

FIG. 39

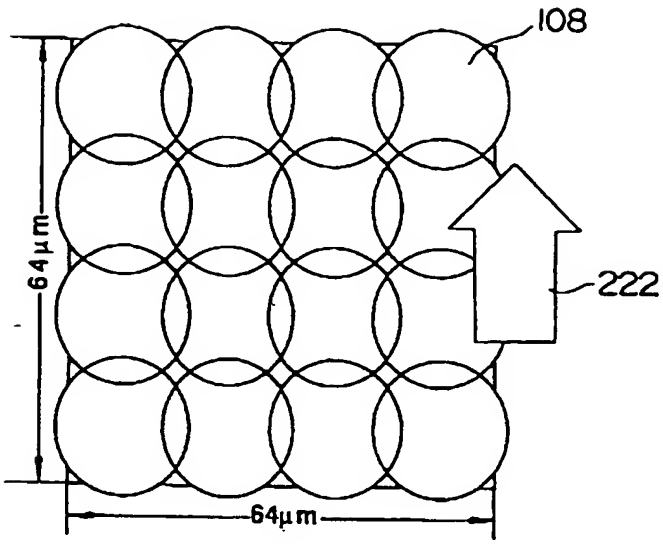


FIG. 40

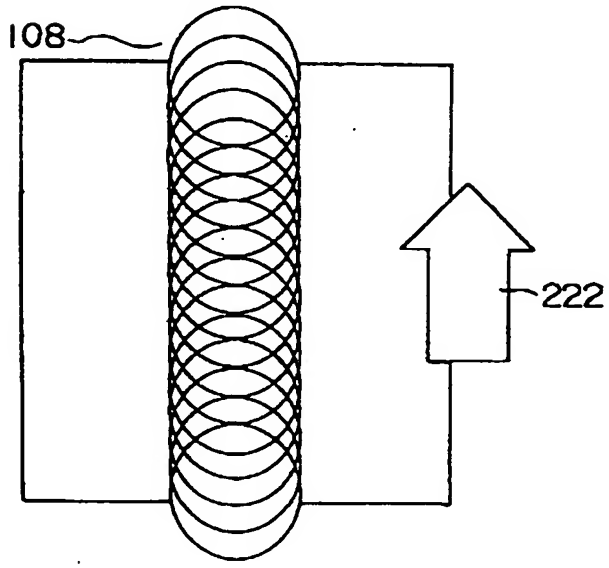


FIG. 41

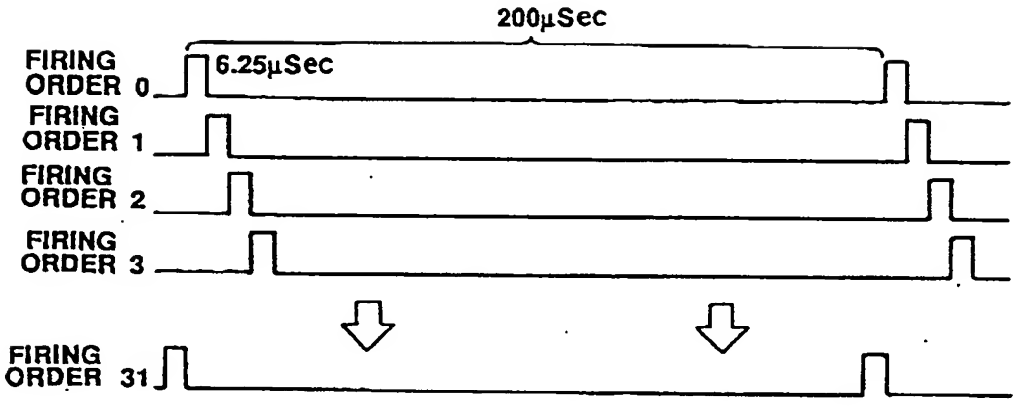

200μSec
6.25μSec
FIRING ORDER 0
FIRING ORDER 1
FIRING ORDER 2
FIRING ORDER 3
FIRING ORDER 31

FIG. 42

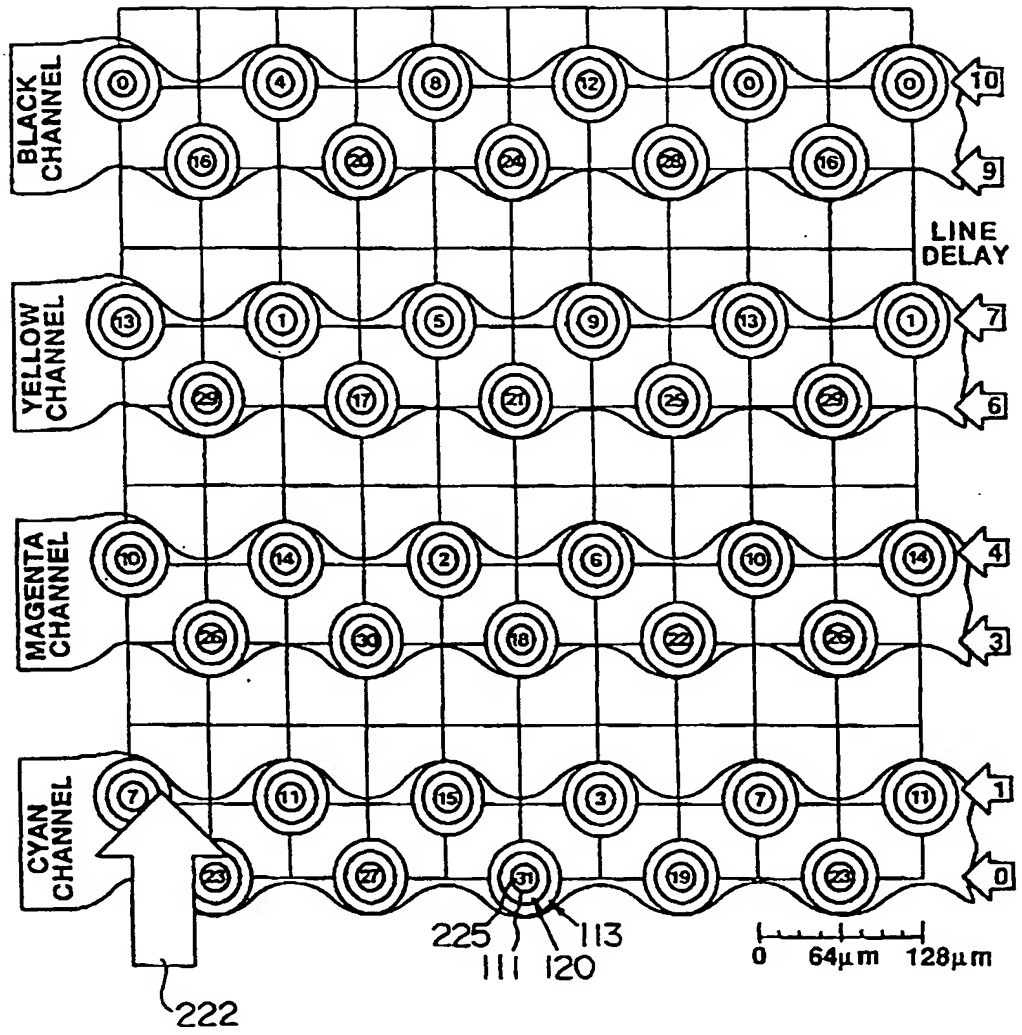

BLACK CHANNEL
YELLOW CHANNEL
MAGENTA CHANNEL
CYAN CHANNEL
LINE DELAY
10
9
7
6
4
3
1
0
222
225
111
120
113
0
64µm
128µm

FIG. 43

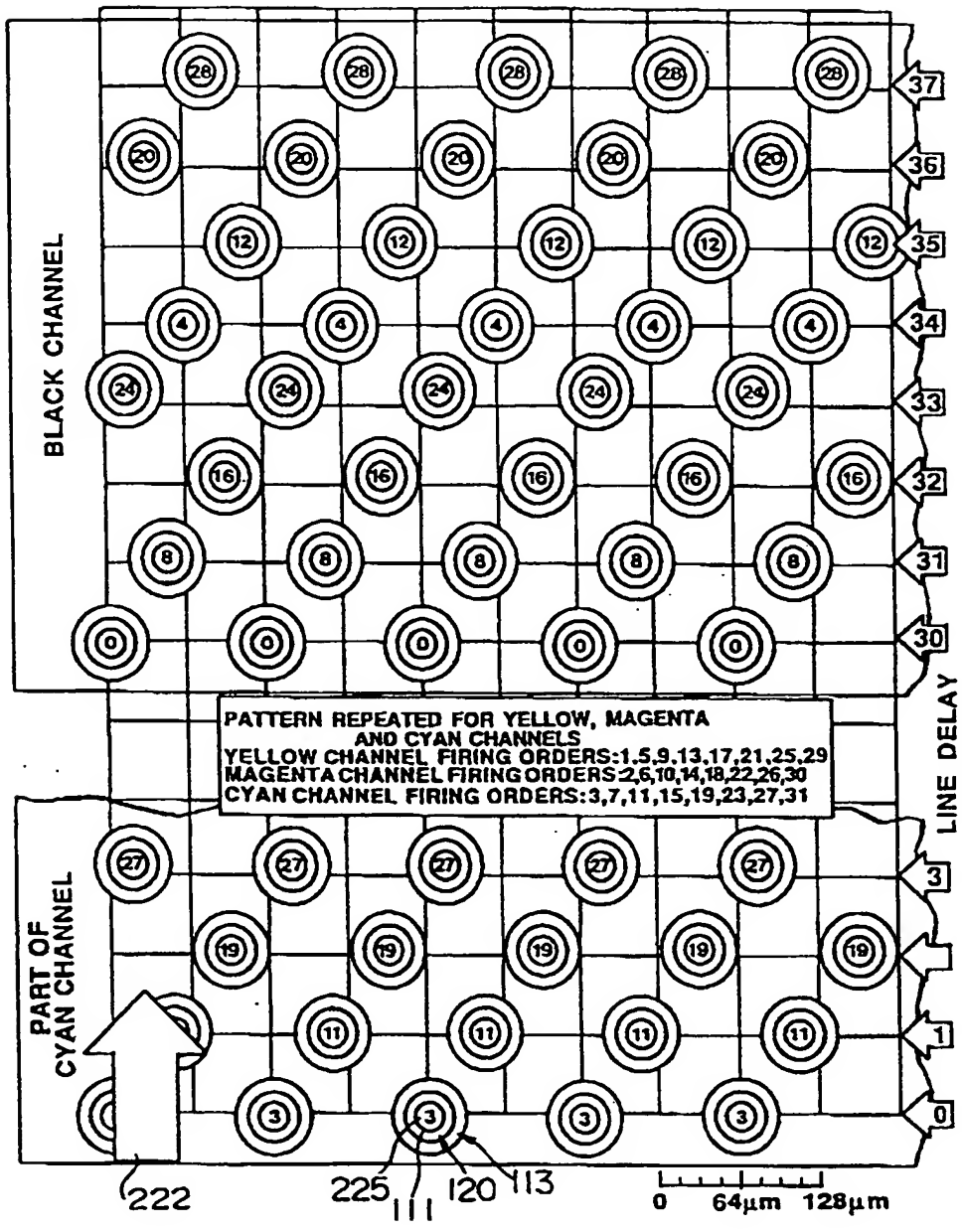

BLACK CHANNEL
PATTERN REPEATED FOR YELLOW, MAGENTA AND CYAN CHANNELS
YELLOW CHANNEL FIRING ORDERS:1,5,9,13,17,21,25,29
MAGENTA CHANNEL FIRING ORDERS:2,6,10,14,18,22,26,30
CYAN CHANNEL FIRING ORDERS:3,7,11,15,19,23,27,31
PART OF CYAN CHANNEL
LINE DELAY
222
225
111
120
113
0
64µm
128µm

FIG.44

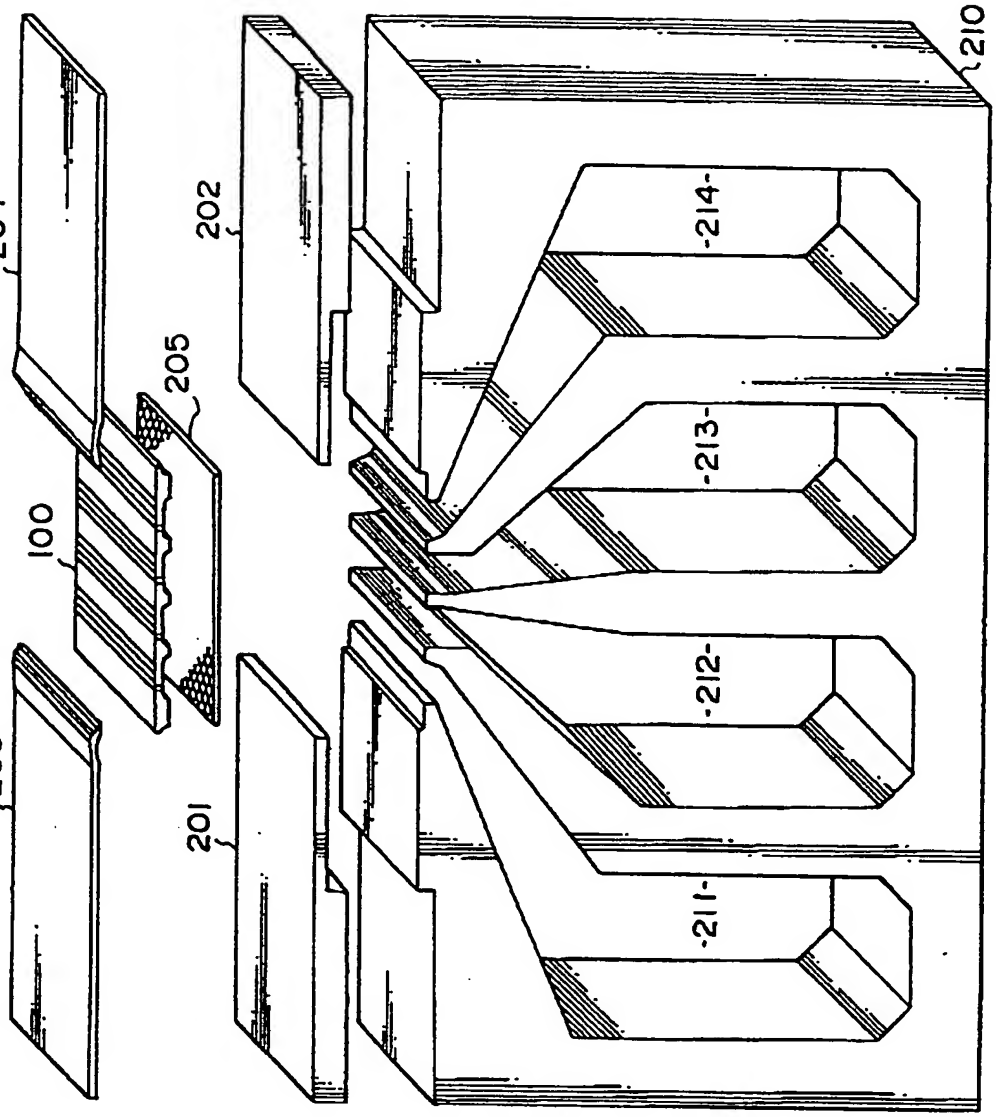


FIG. 46

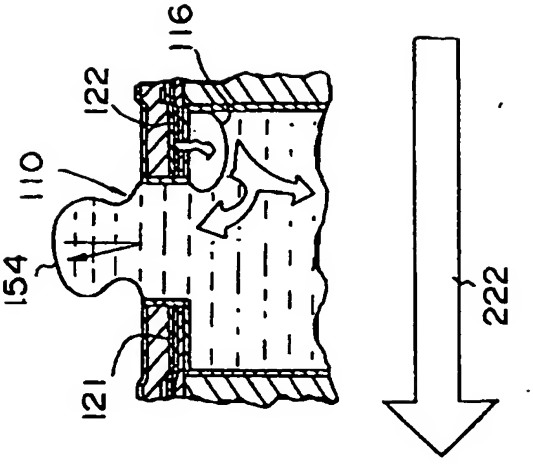
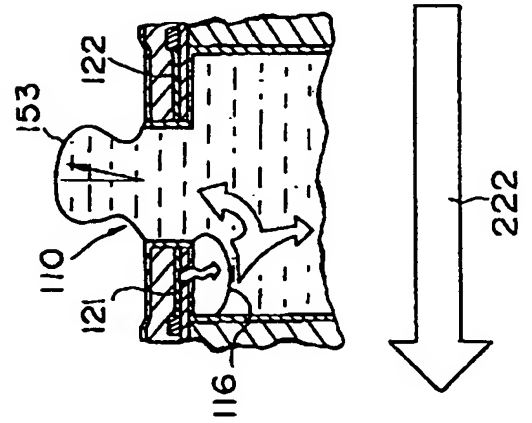


FIG. 45



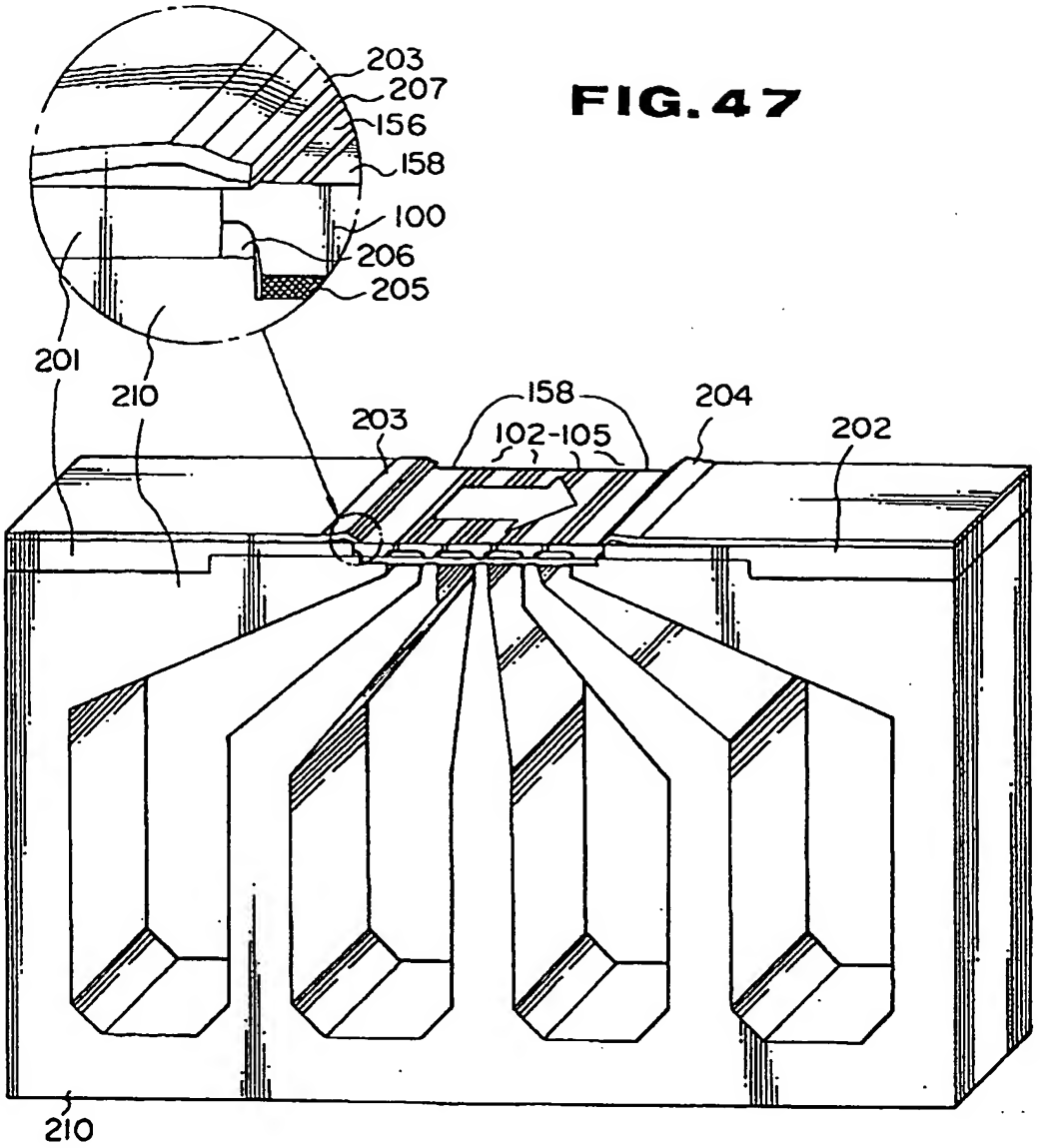

203
207
156
158
100
206
205
201
210
203
158
102-105
204
202
210

FIG. 47

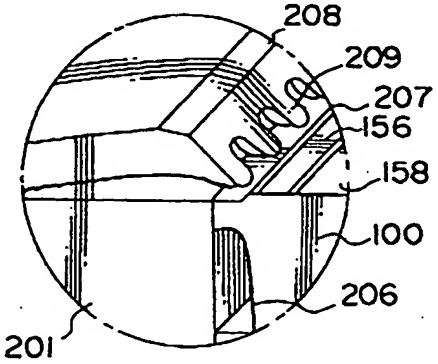

208
209
207
156
158
100
206
201

FIG. 48

FIG.49
(PRIOR ART)

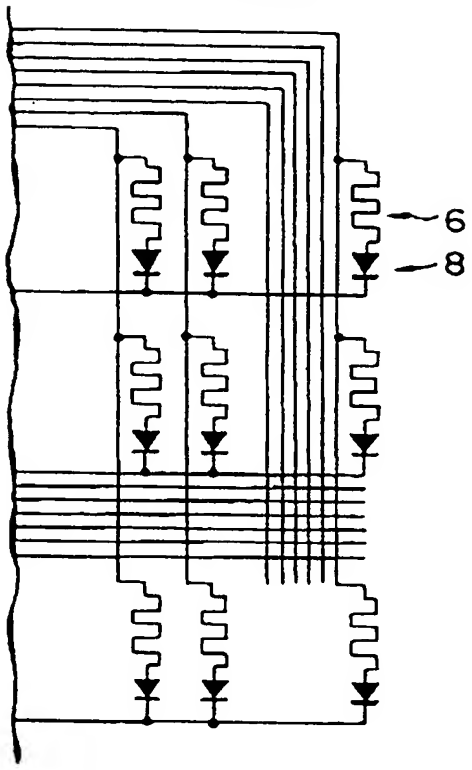


FIG.51

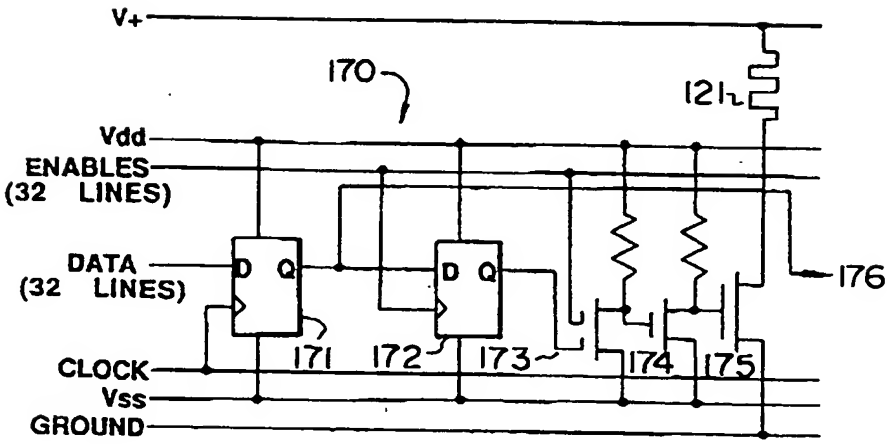


FIG.50

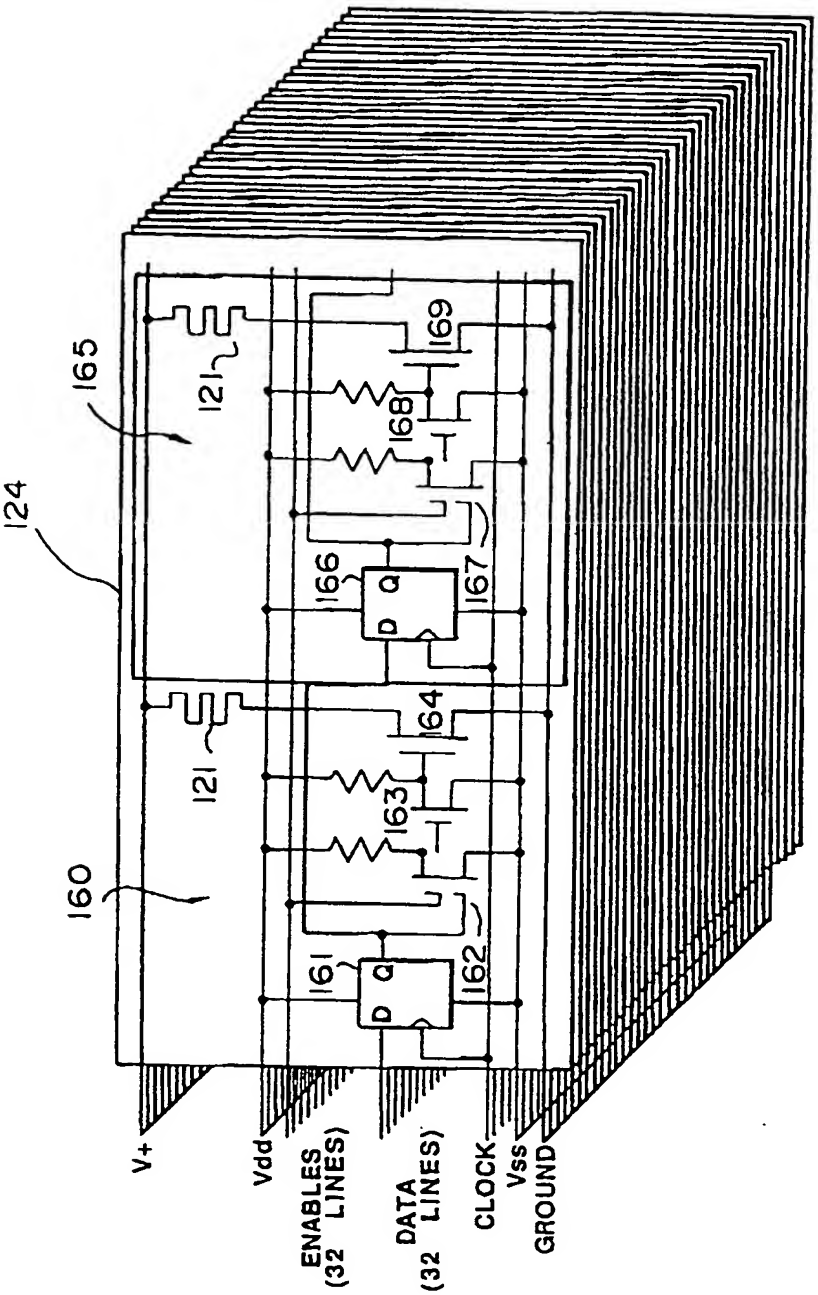

124
165
160
121
121
169
168
166
167
164
163
161
162
D Q
D Q
V+
Vdd
ENABLES (32 LINES)
DATA (32 LINES)
CLOCK
Vss
GROUND

FIG. 52

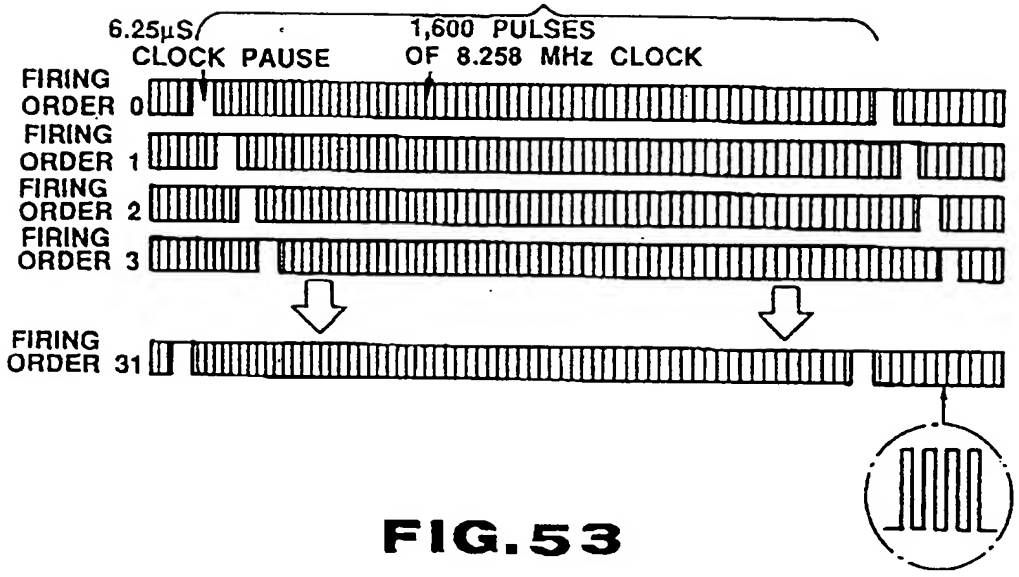

6.25μS
CLOCK PAUSE
1,600 PULSES
OF 8.258 MHz CLOCK
FIRING ORDER 0
FIRING ORDER 1
FIRING ORDER 2
FIRING ORDER 3
FIRING ORDER 31

FIG. 53

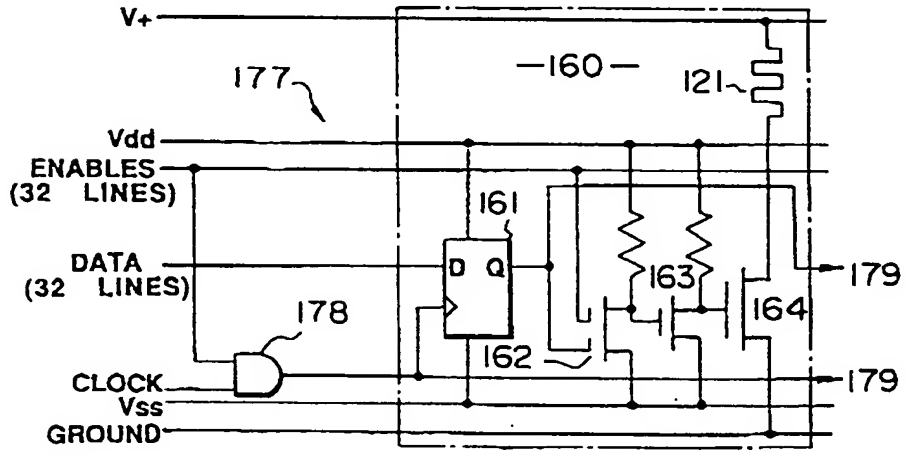

V+
177
160
121
Vdd
ENABLES (32 LINES)
161
DATA (32 LINES)
D Q
163
164
179
178
162
CLOCK
179
Vss
GROUND

FIG.54

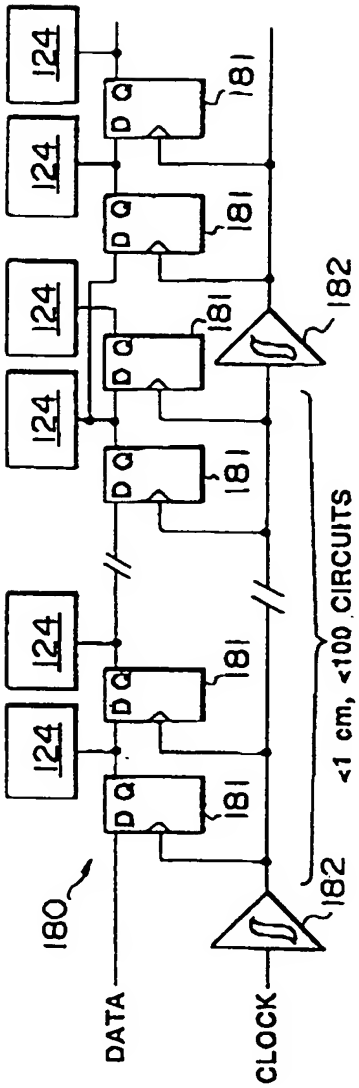

124
181
180
182
DATA
CLOCK
<1 cm, <100 CIRCUITS

FIG.55

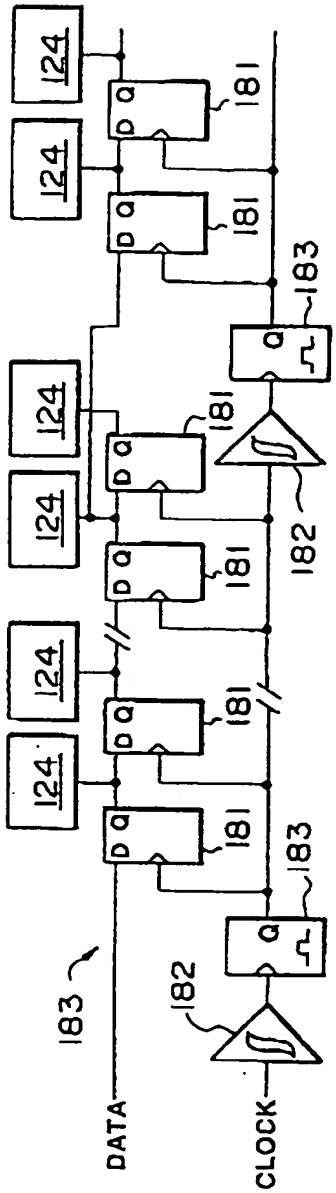

124
181
183
182
183
DATA
CLOCK

FIG.56

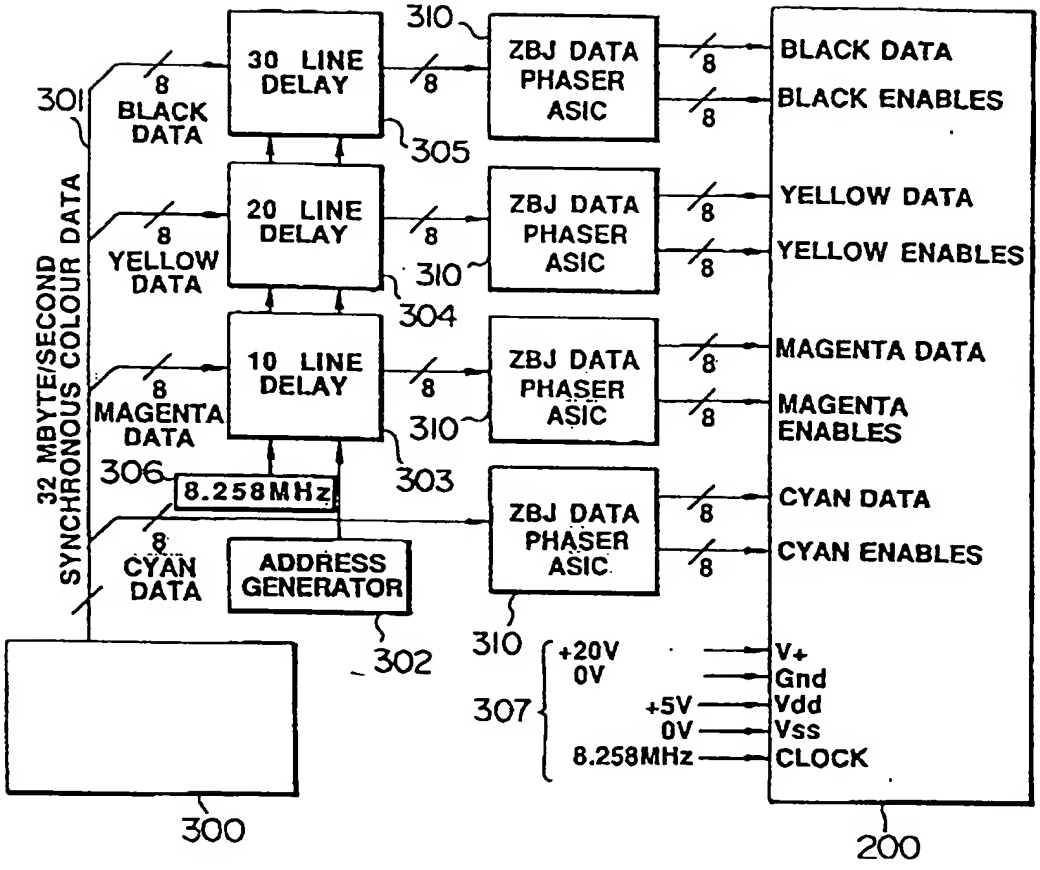

30 LINE DELAY
20 LINE DELAY
10 LINE DELAY
8.258MHz
ADDRESS GENERATOR
ZBJ DATA PHASER ASIC
ZBJ DATA PHASER ASIC
ZBJ DATA PHASER ASIC
ZBJ DATA PHASER ASIC
8 BLACK DATA
8 YELLOW DATA
8 MAGENTA DATA
8 CYAN DATA
32 MBYTE/SECOND SYNCHRONOUS COLOUR DATA
BLACK DATA
BLACK ENABLES
YELLOW DATA
YELLOW ENABLES
MAGENTA DATA
MAGENTA ENABLES
CYAN DATA
CYAN ENABLES
+20V
0V
+5V
0V
8.258MHz
V+
Gnd
Vdd
Vss
CLOCK
300
301
302
303
304
305
306
307
310
200

FIG.57

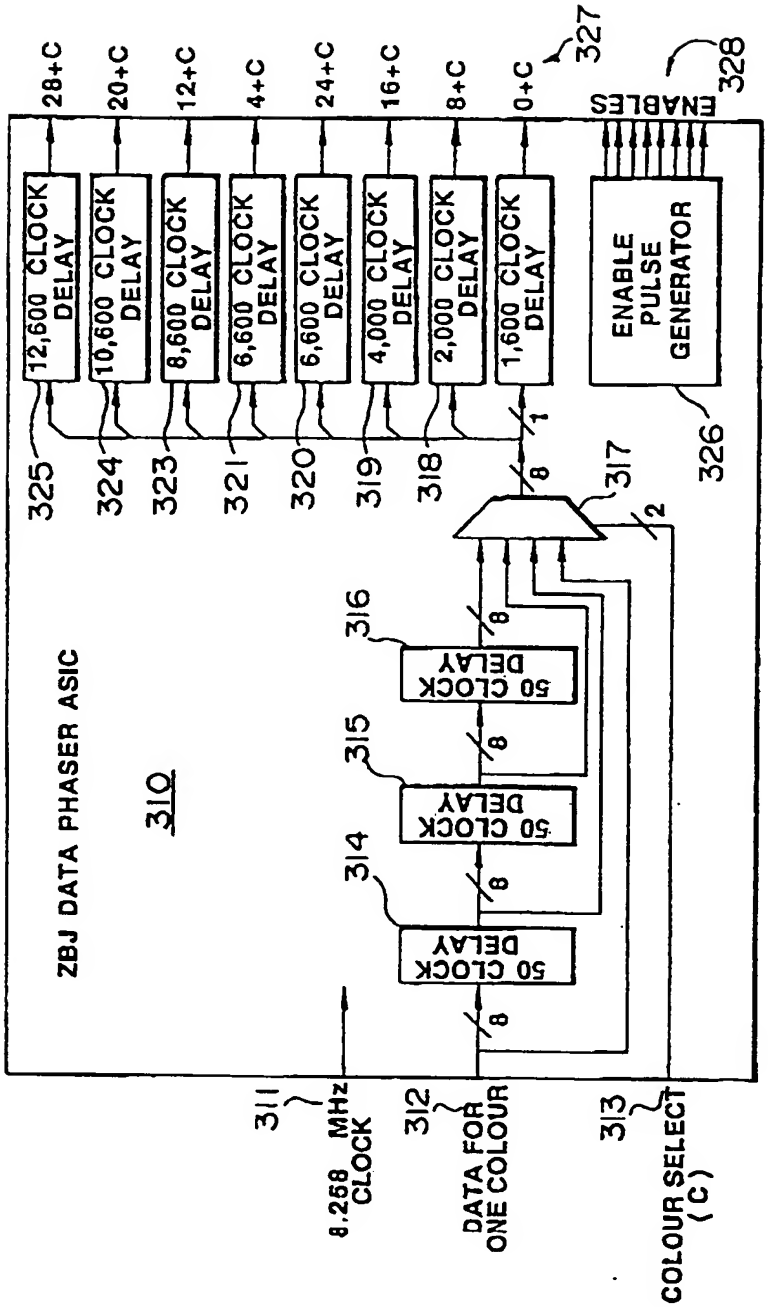

ZBJ DATA PHASER ASIC
310
12,600 CLOCK DELAY
10,600 CLOCK DELAY
8,600 CLOCK DELAY
6,600 CLOCK DELAY
6,600 CLOCK DELAY
4,000 CLOCK DELAY
2,000 CLOCK DELAY
1,600 CLOCK DELAY
ENABLE PULSE GENERATOR
50 CLOCK DELAY
50 CLOCK DELAY
50 CLOCK DELAY
28+C
20+C
12+C
4+C
24+C
16+C
8+C
0+C
ENABLES
325
324
323
321
320
319
318
317
316
315
314
326
327
328
311
312
313
8.268 MHz CLOCK
DATA FOR ONE COLOUR
COLOUR SELECT (C)

FIG.58(a)

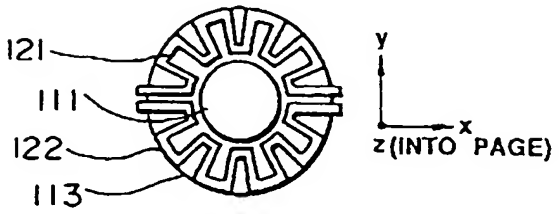


FIG.58(b)

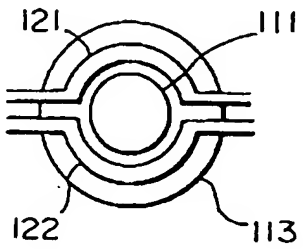


FIG.59

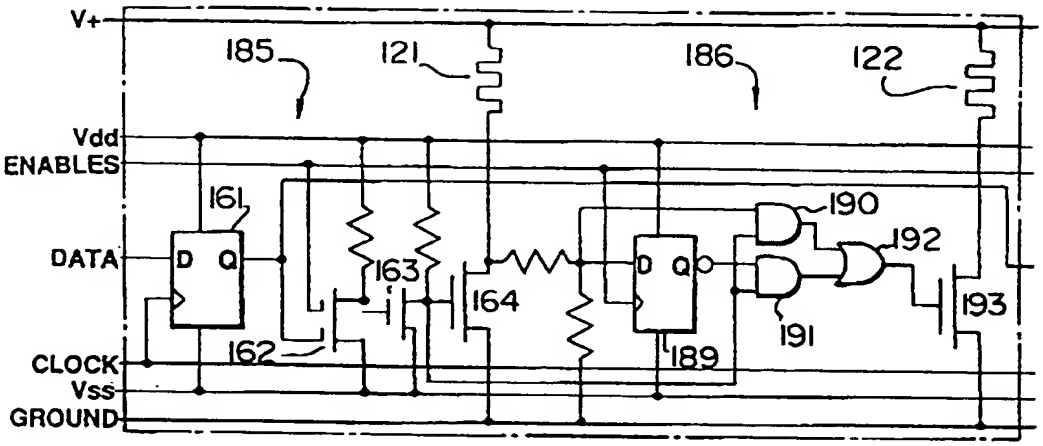


FIG.60

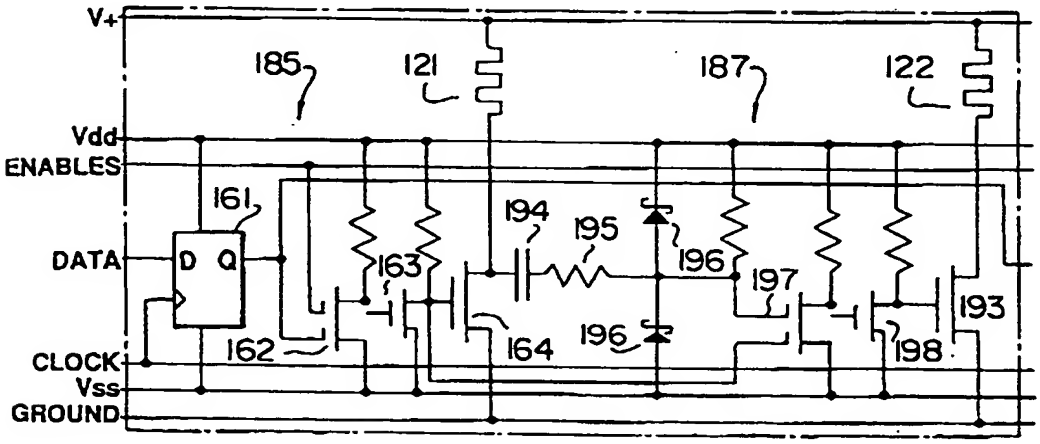


FIG.61

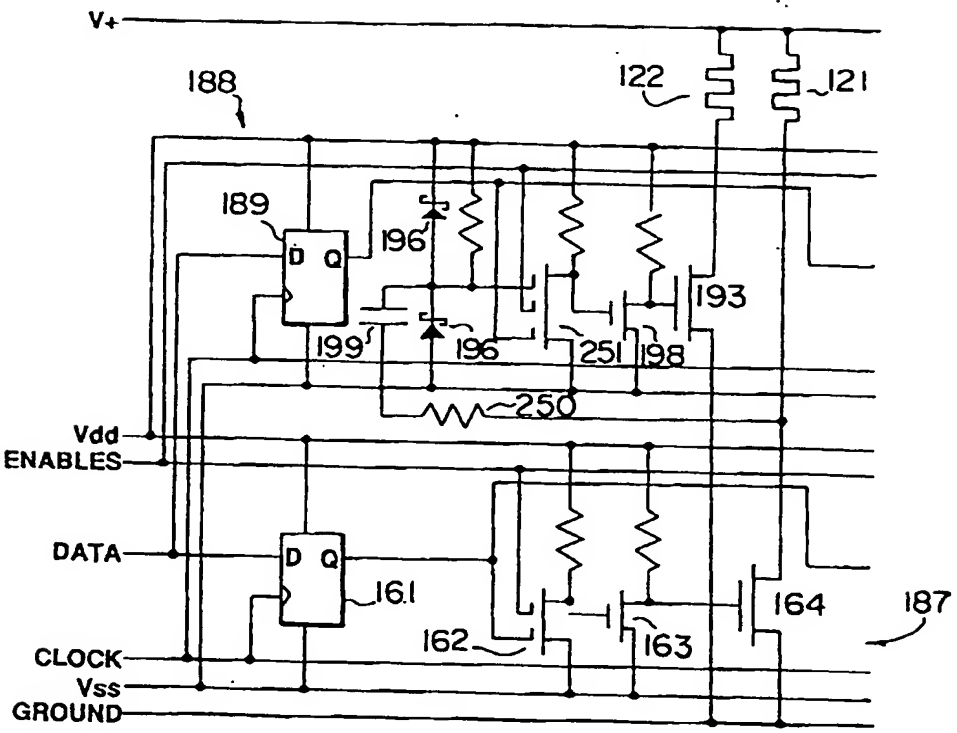

V+
188
122
121
189
D Q
196
193
199
196
251
198
250
Vdd
ENABLES
DATA
D Q
161
164
187
162
163
CLOCK
Vss
GROUND

FIG.62

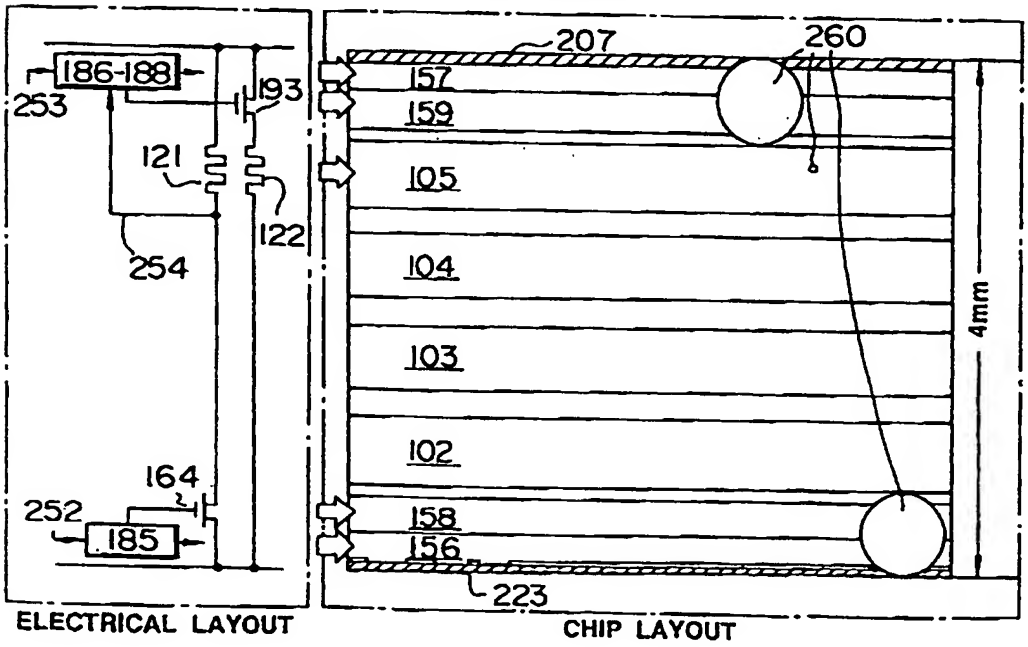

186-188
253
193
121
122
254
164
252
185
207
260
157
159
105
104
103
102
158
156
223
4mm
ELECTRICAL LAYOUT
CHIP LAYOUT

FIG.63

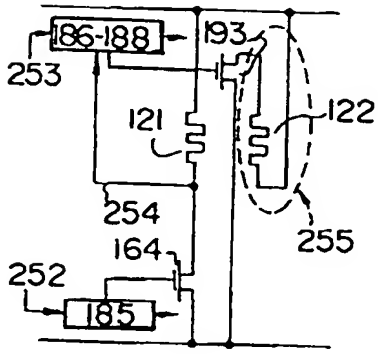

186-188
193
253
121
122
254
255
164
252
185

FIG.64

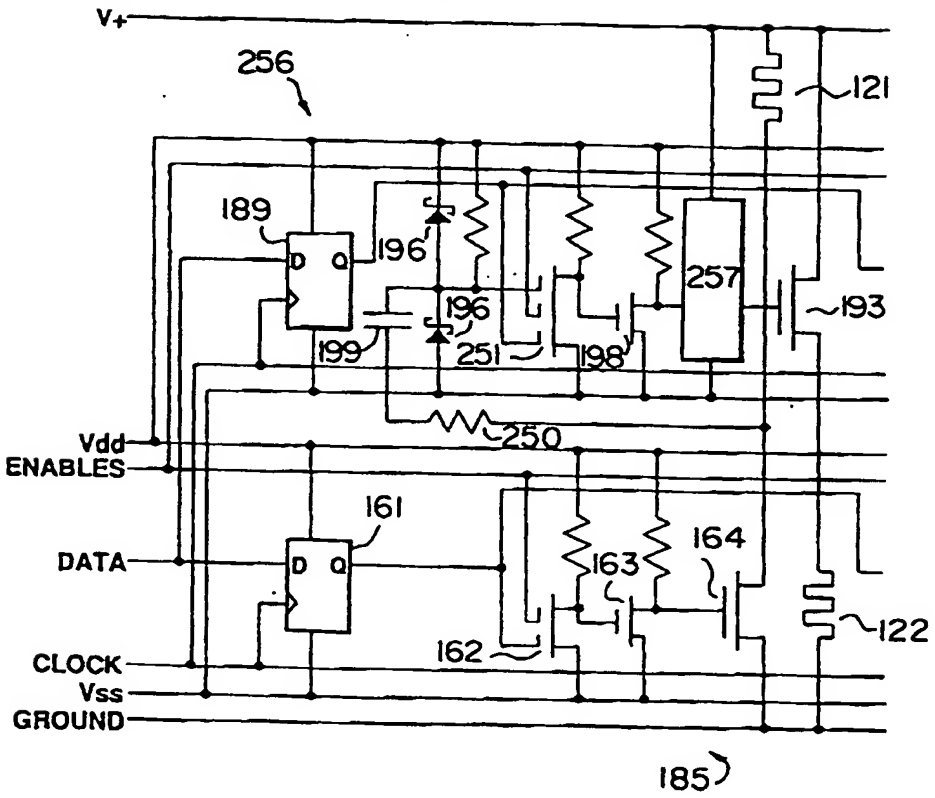

V+
256
121
189
D Q
196
196
257
193
199
251
198
250
Vdd
ENABLES
161
DATA
D Q
163
164
122
162
CLOCK
Vss
GROUND
185

FIG.65

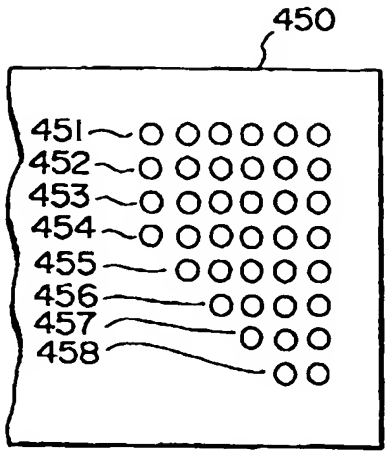


FIG.66

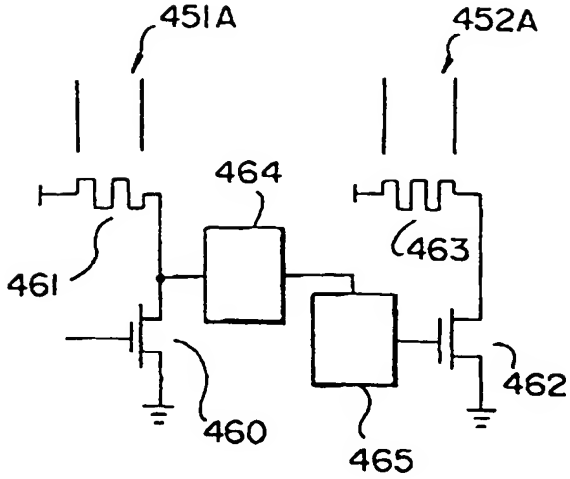


FIG.67

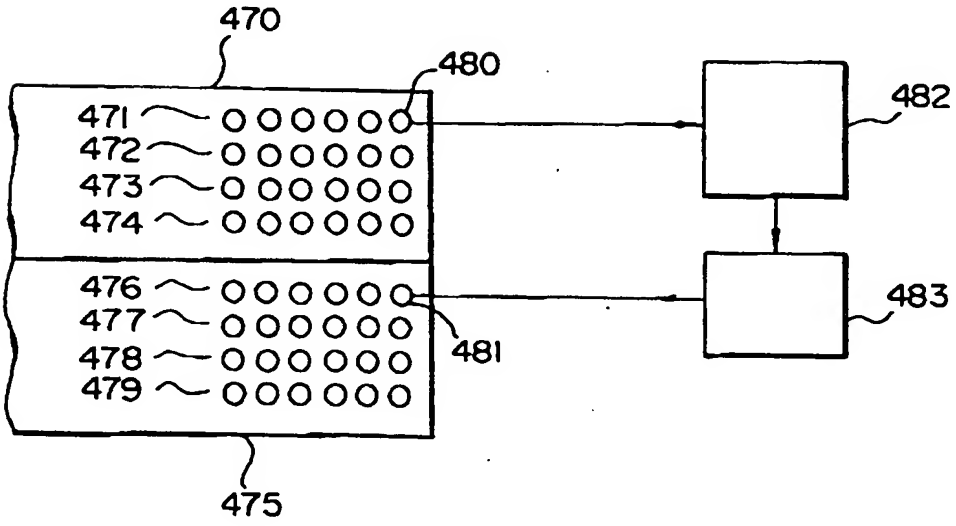


FIG.68

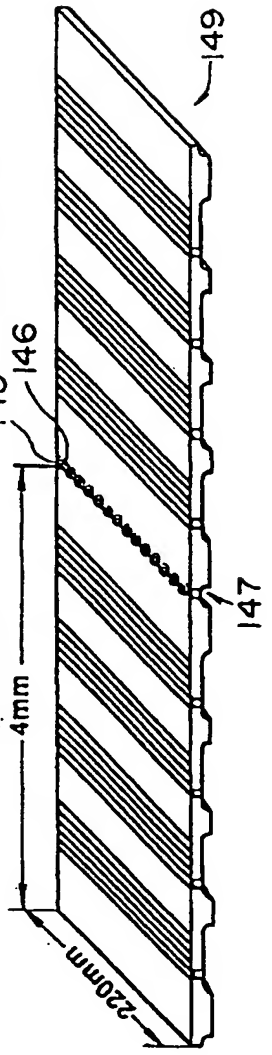

ZBJ CHIP 1
4mm
ZBJ CHIP 2
145
146
147
149
220mm

FIG.69

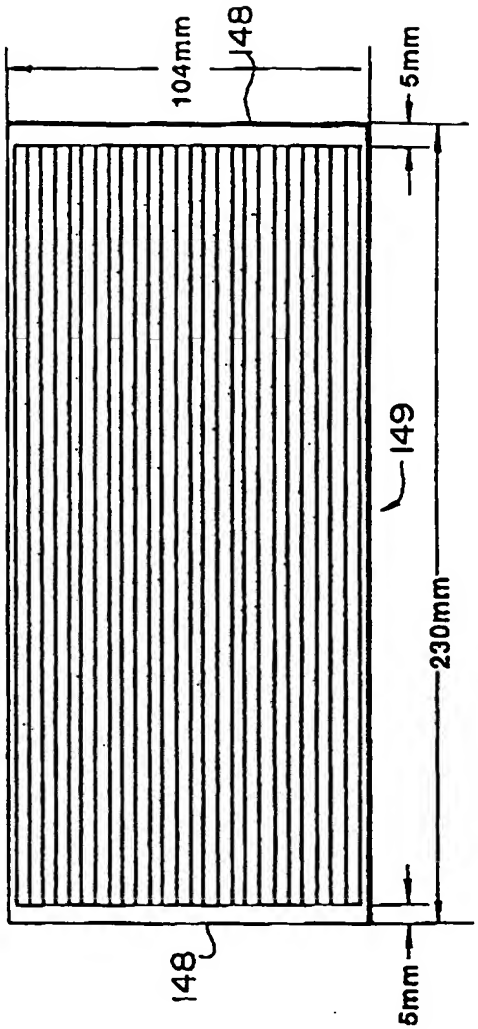

104mm
148
5mm
149
230mm
148
5mm

FIG.70

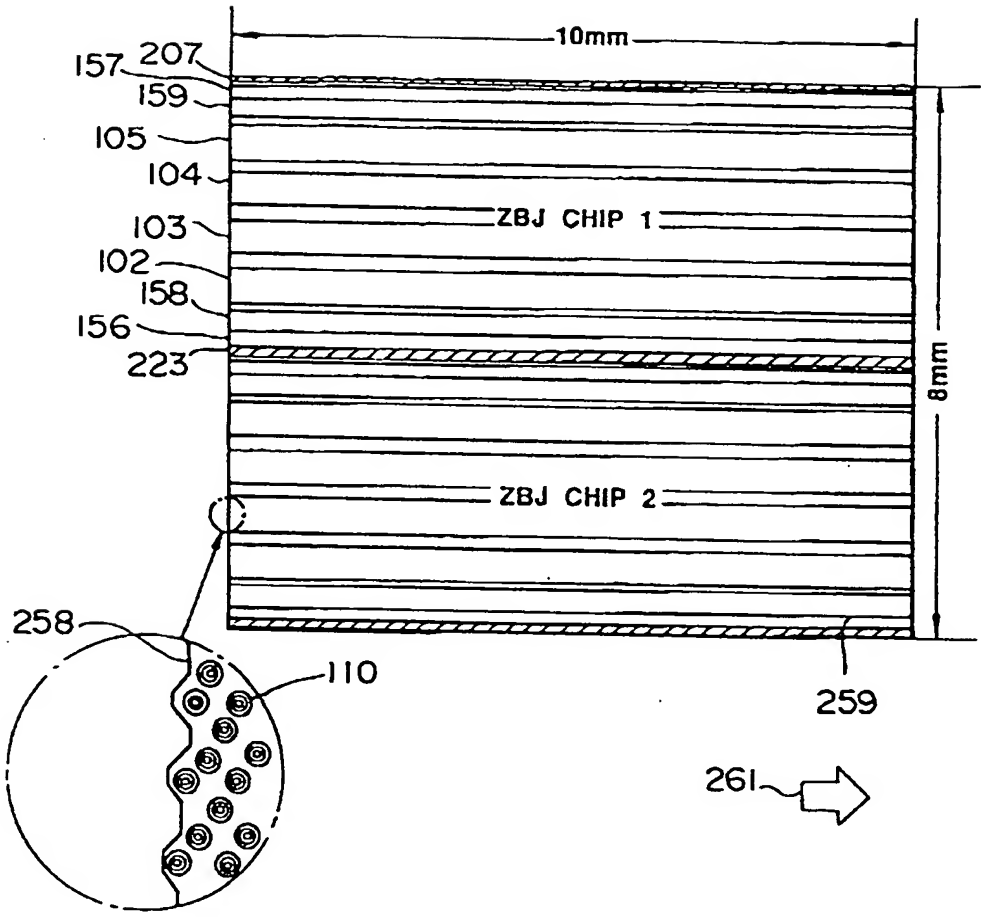

10mm
157
207
159
105
104
103
102
158
156
223
ZBJ CHIP 1
ZBJ CHIP 2
8mm
258
110
259
261

FIG.71

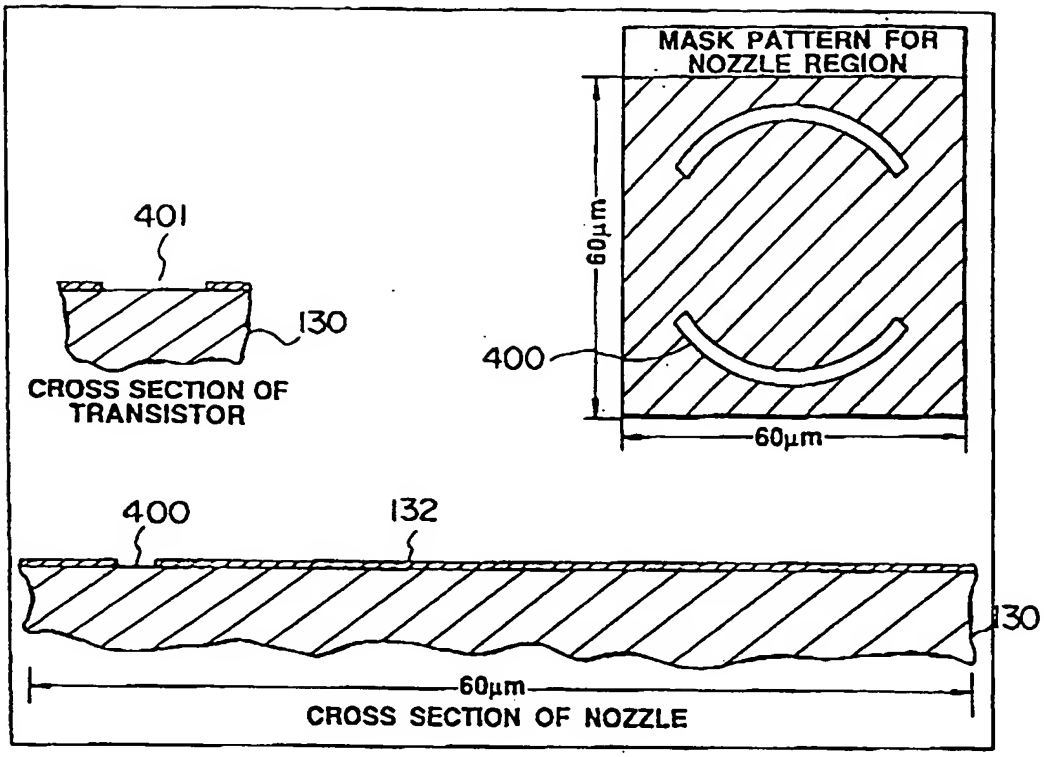

MASK PATTERN FOR NOZZLE REGION
401
130
CROSS SECTION OF TRANSISTOR
60µm
400
60µm
400
132
130
60µm
CROSS SECTION OF NOZZLE

FIG.72

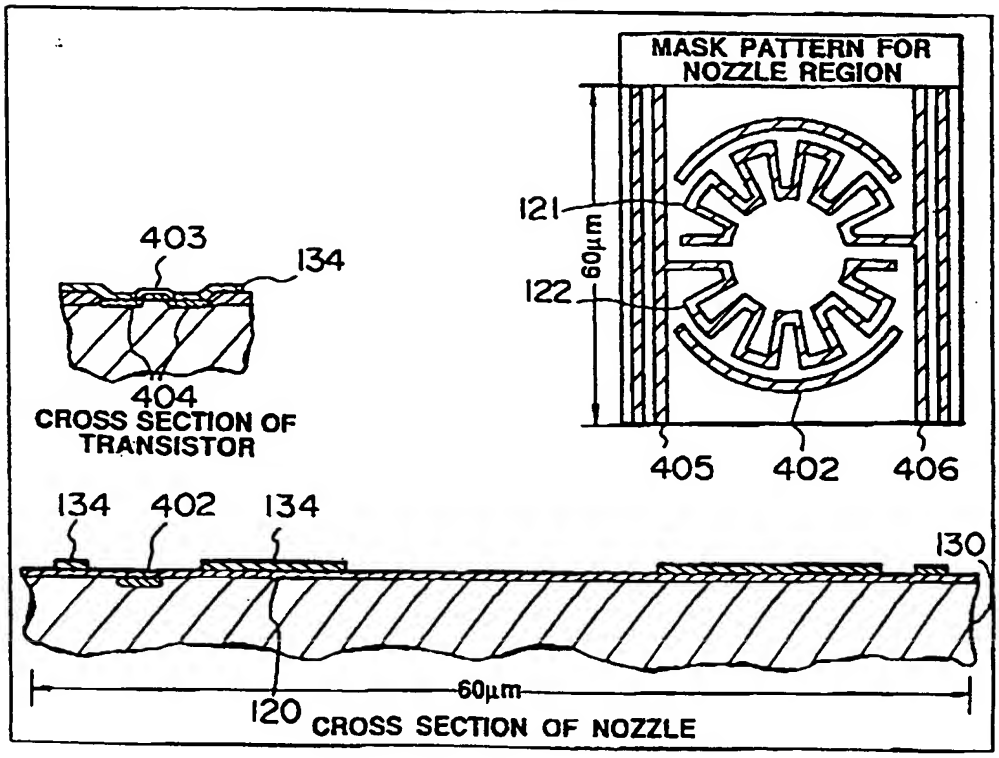

MASK PATTERN FOR NOZZLE REGION
403
134
404
CROSS SECTION OF TRANSISTOR
121
122
60µm
405
402
406
134
402
134
130
60µm
120
CROSS SECTION OF NOZZLE

FIG.73

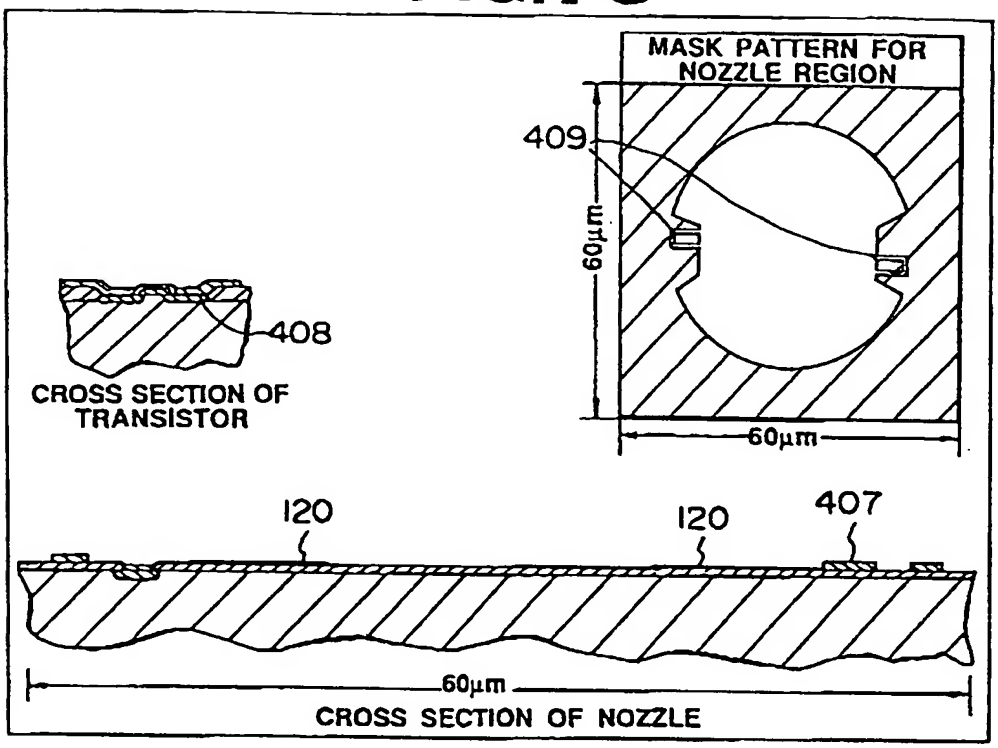

MASK PATTERN FOR NOZZLE REGION
409
60μm
60μm
408
CROSS SECTION OF TRANSISTOR
120
120
407
60μm
CROSS SECTION OF NOZZLE

FIG.74

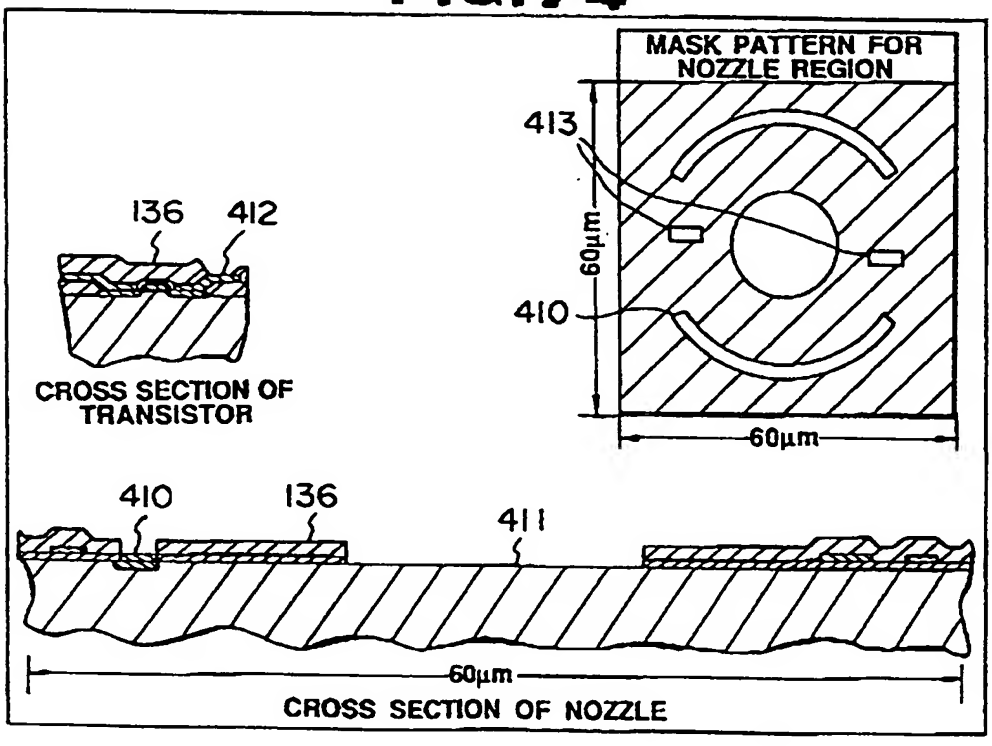

MASK PATTERN FOR NOZZLE REGION
413
60μm
410
60μm
136
412
CROSS SECTION OF TRANSISTOR
410
136
411
60μm
CROSS SECTION OF NOZZLE

FIG.75

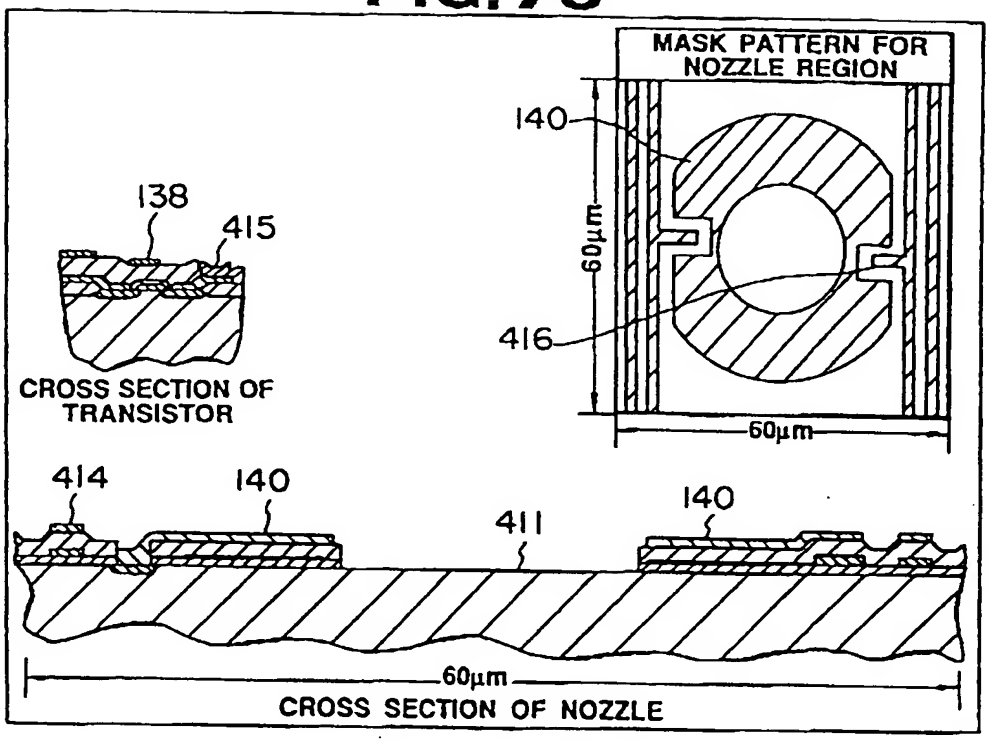

MASK PATTERN FOR NOZZLE REGION
140
60μm
416
60μm
138
415
CROSS SECTION OF TRANSISTOR
414
140
411
140
60μm
CROSS SECTION OF NOZZLE

FIG.76

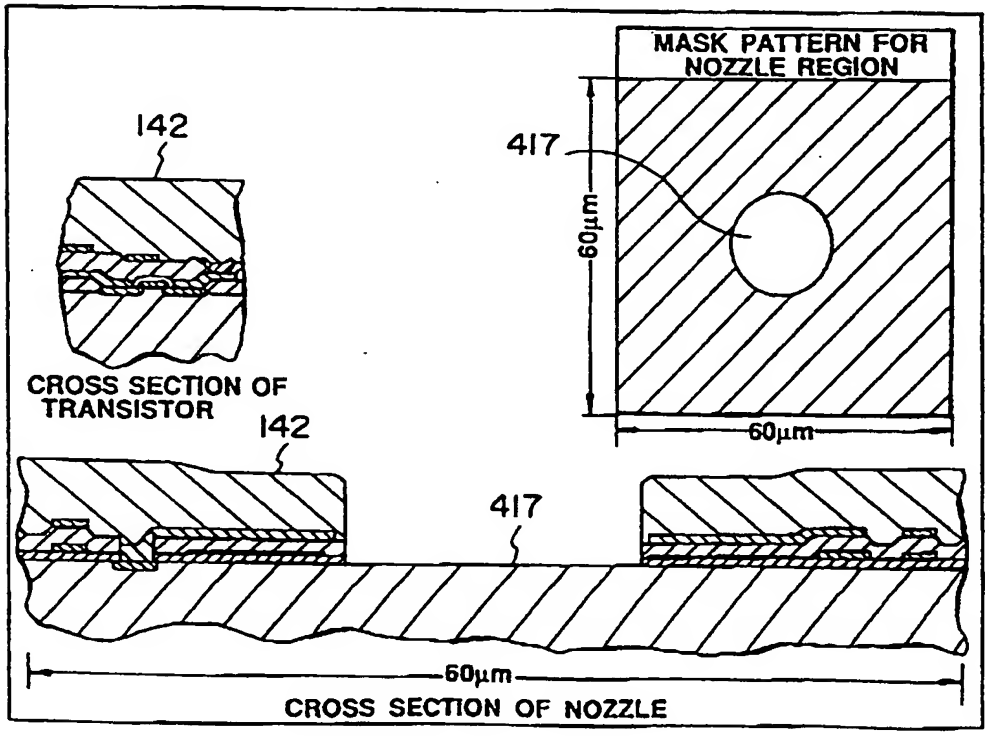

MASK PATTERN FOR NOZZLE REGION
417
60μm
60μm
142
CROSS SECTION OF TRANSISTOR
142
417
60μm
CROSS SECTION OF NOZZLE

FIG.77

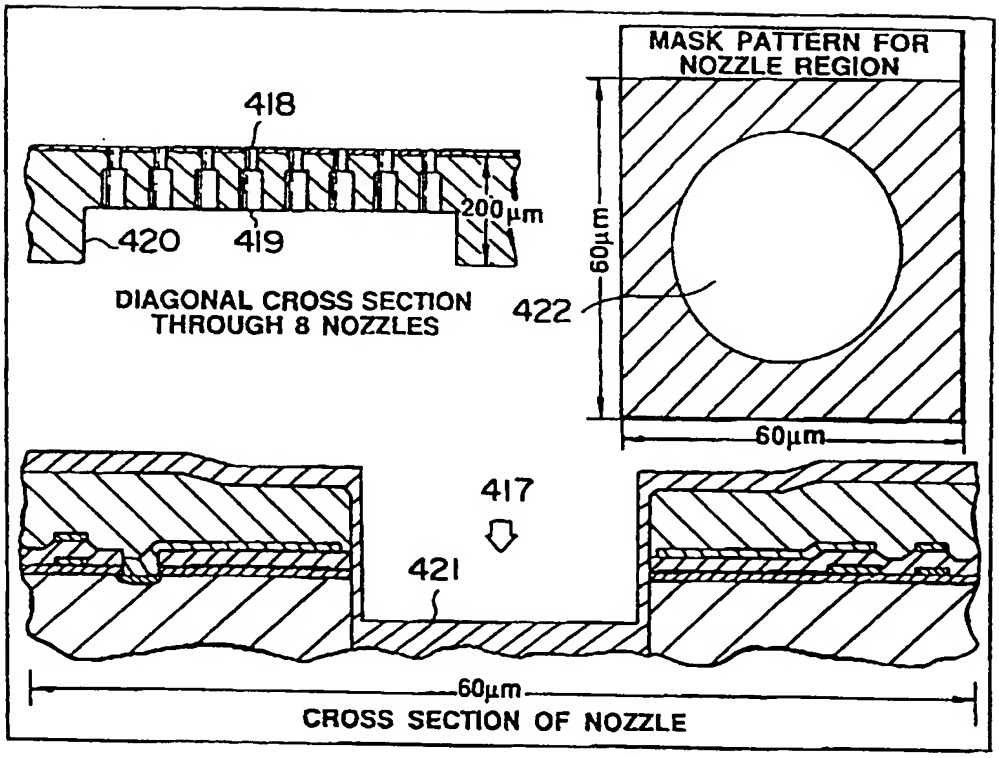

MASK PATTERN FOR NOZZLE REGION
418
200µm
420
419
DIAGONAL CROSS SECTION THROUGH 8 NOZZLES
422
60µm
60µm
417
421
60µm
CROSS SECTION OF NOZZLE

FIG.78

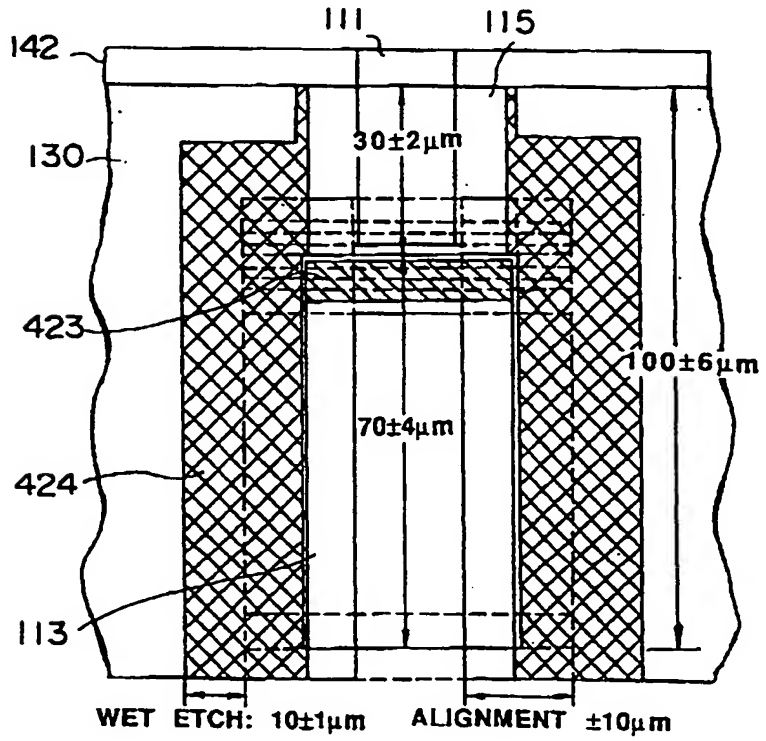

111
115
142
130
30±2µm
423
100±6µm
70±4µm
424
113
WET ETCH: 10±1µm
ALIGNMENT ±10µm

FIG.79

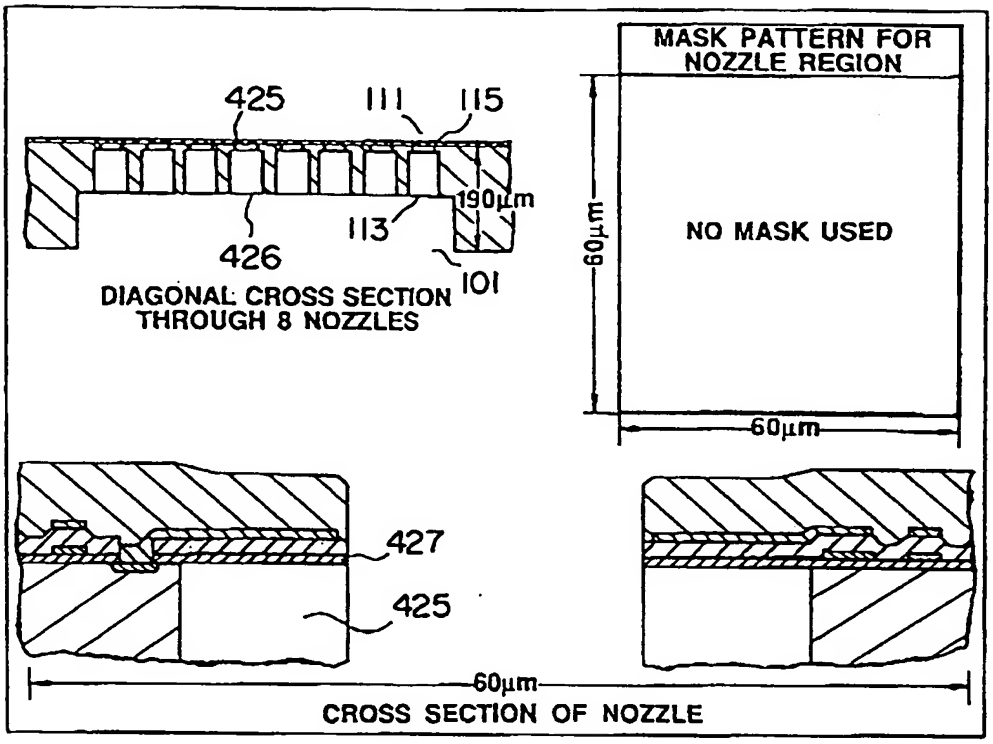

MASK PATTERN FOR NOZZLE REGION
425
111
115
190µm
113
426
101
DIAGONAL CROSS SECTION THROUGH 8 NOZZLES
60µm
NO MASK USED
60µm
427
425
60µm
CROSS SECTION OF NOZZLE

FIG.80

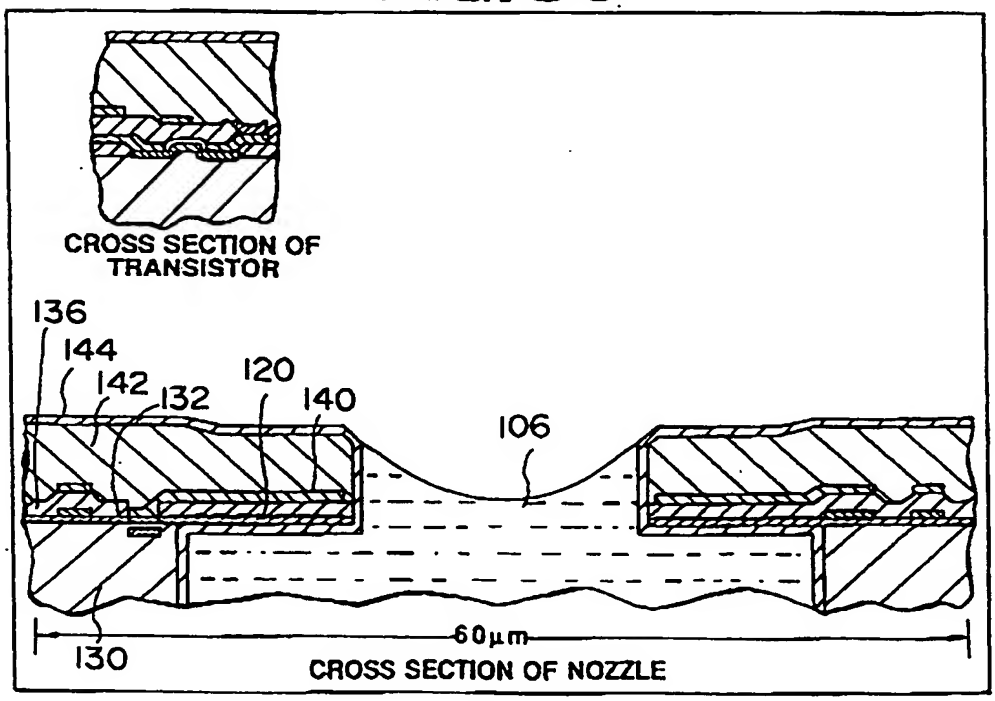

CROSS SECTION OF TRANSISTOR
136
144
142
132
120
140
106
130
60µm
CROSS SECTION OF NOZZLE

FIG. 81

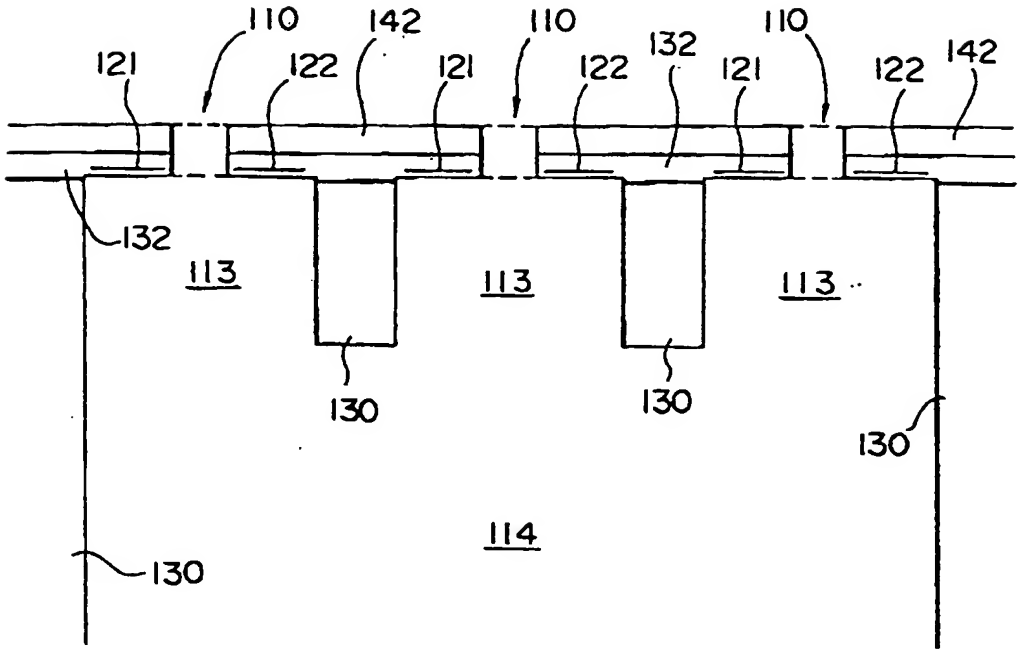

110
142
110
132
110
121
122
121
122
121
122
142
132
113
113
113
130
130
130
114
130

FIG.82

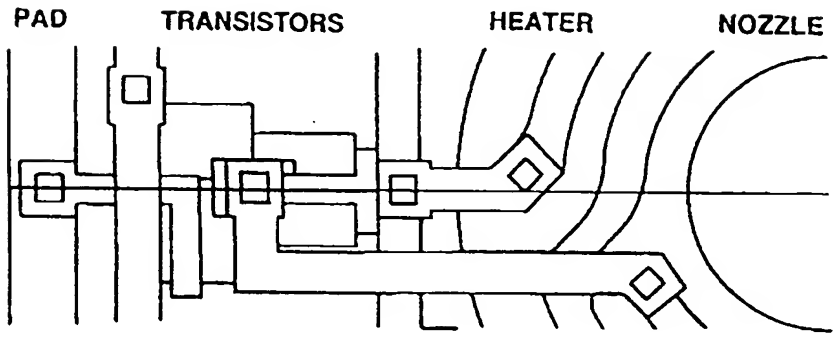


FIG.83

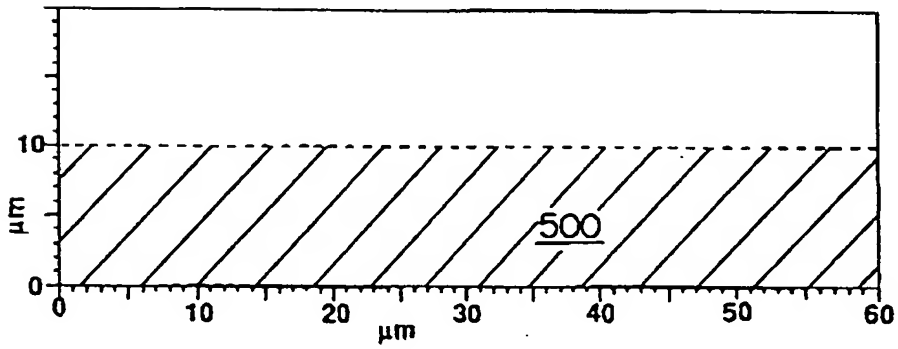


FIG.84

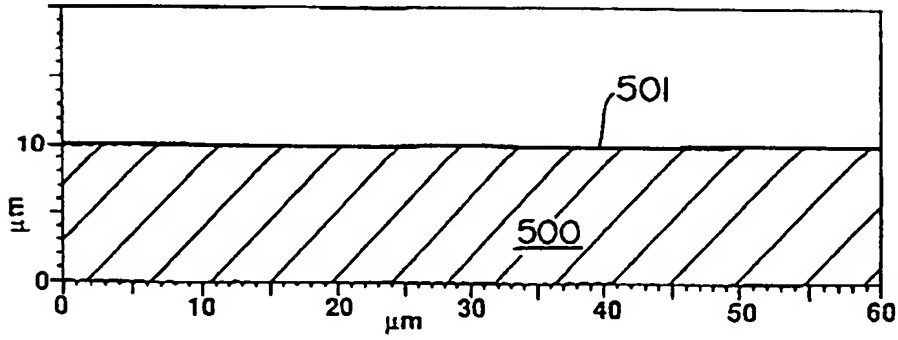


FIG.85

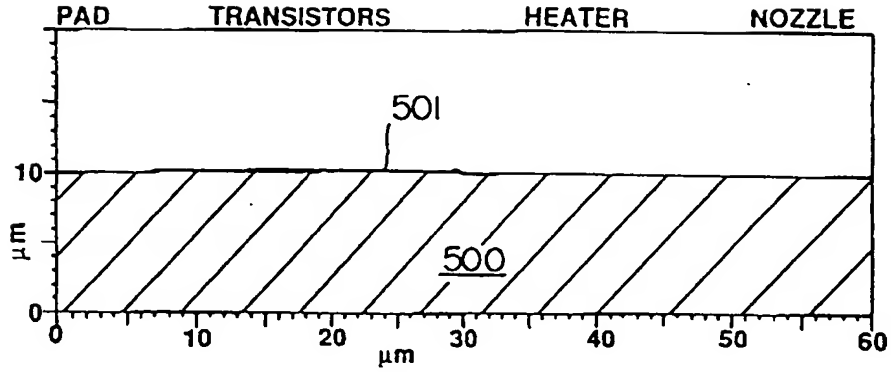


FIG.86

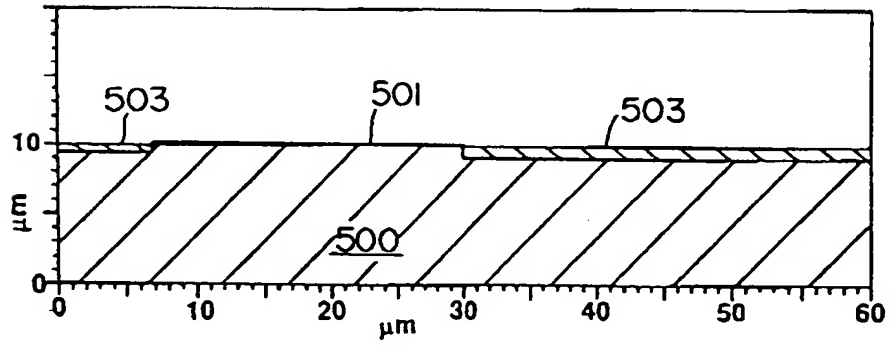


FIG.87

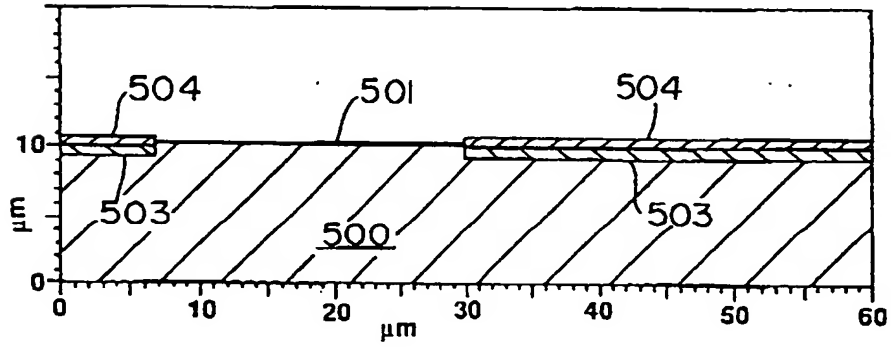


FIG.88

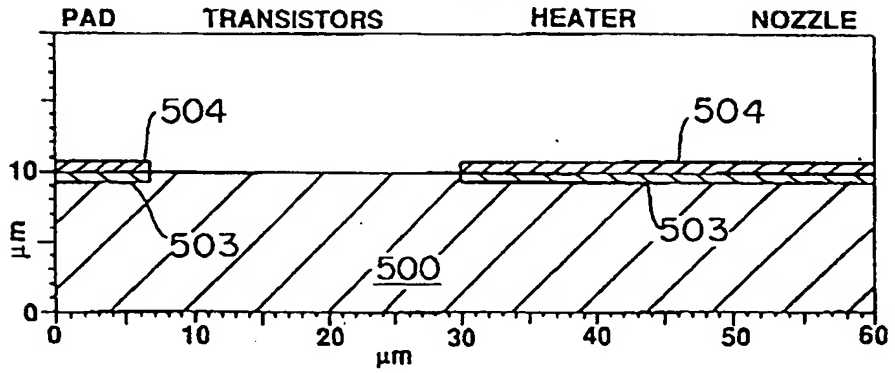


FIG.89

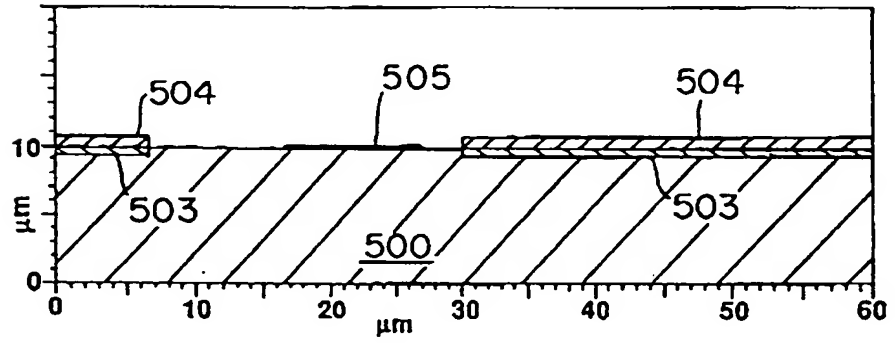


FIG.90

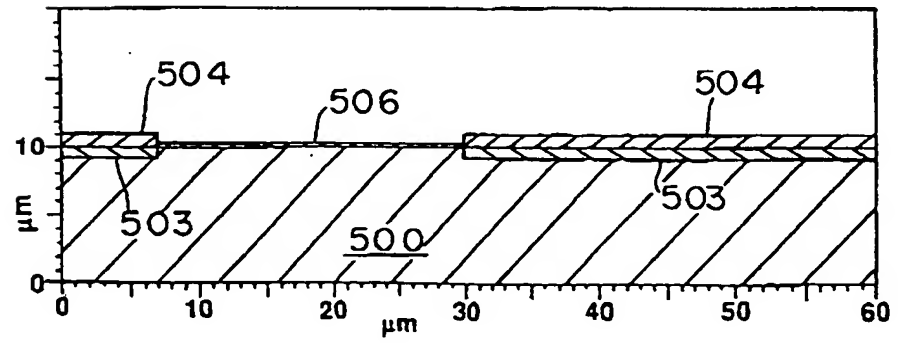


FIG.91

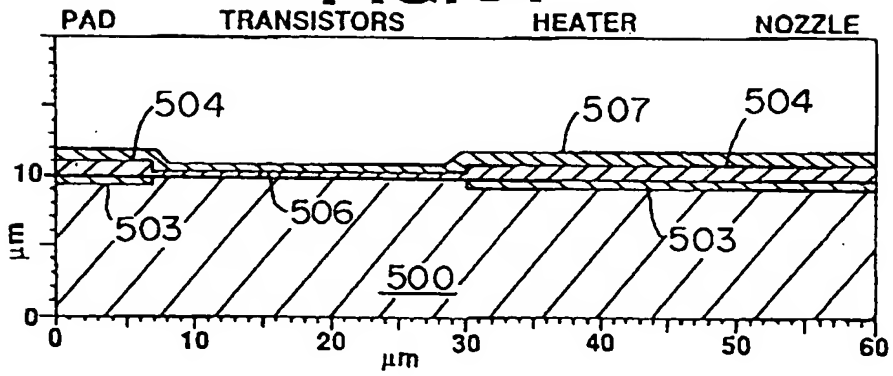


FIG.92

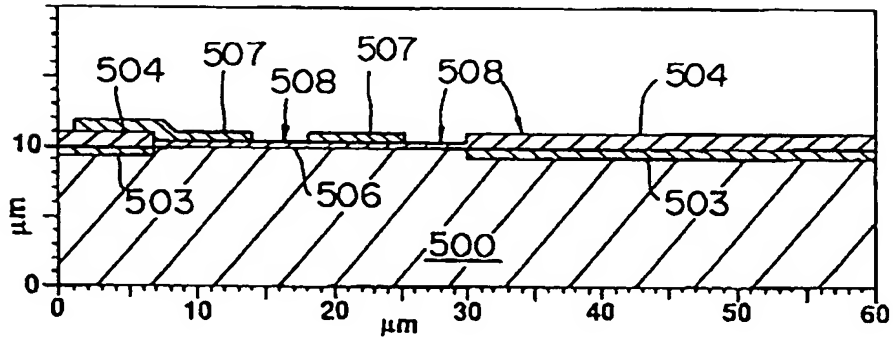


FIG.93

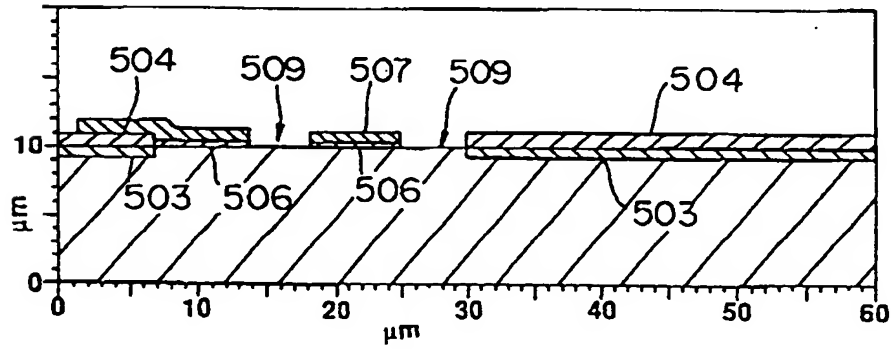


FIG. 94

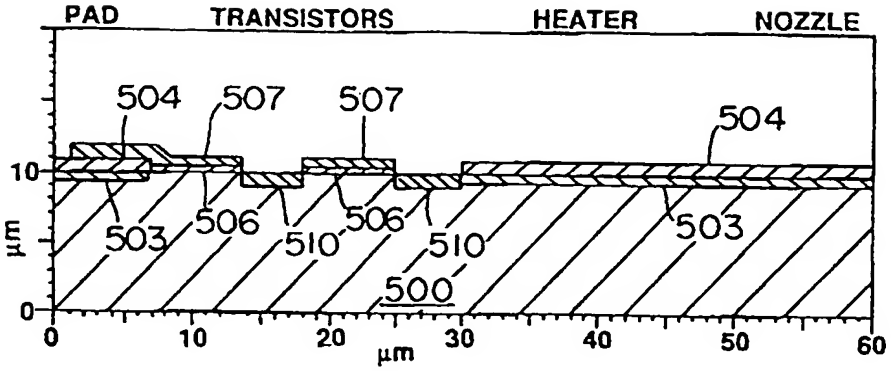


FIG. 95

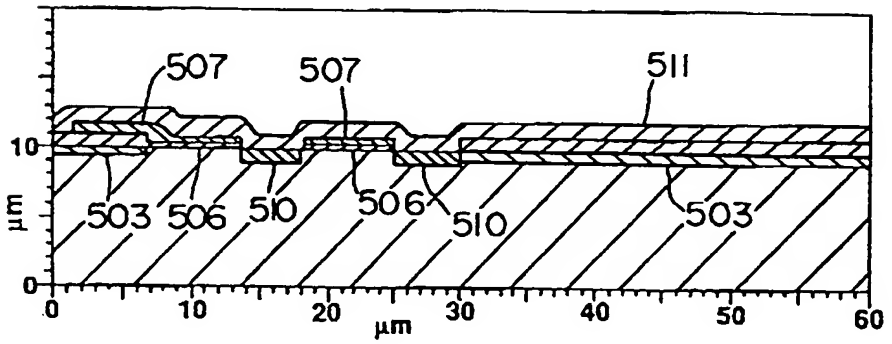


FIG. 96

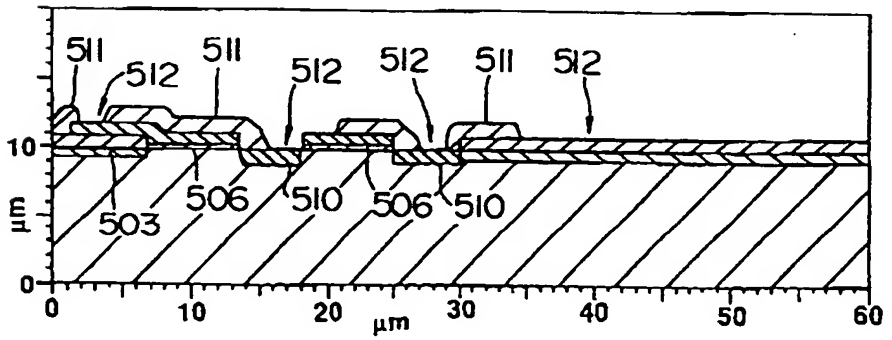


FIG.97

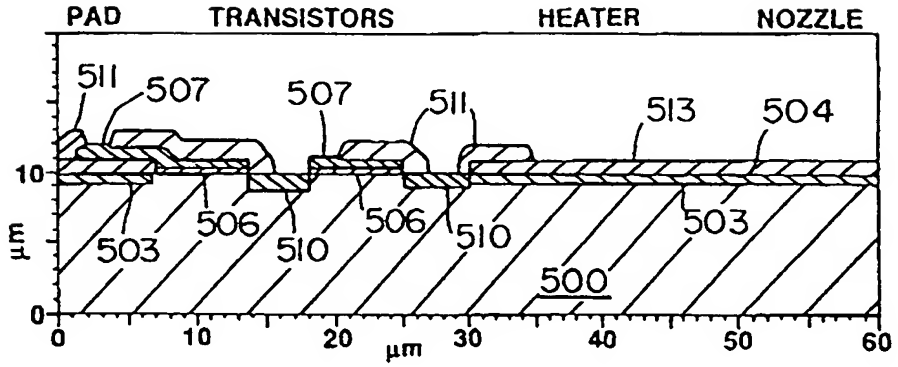


FIG.98

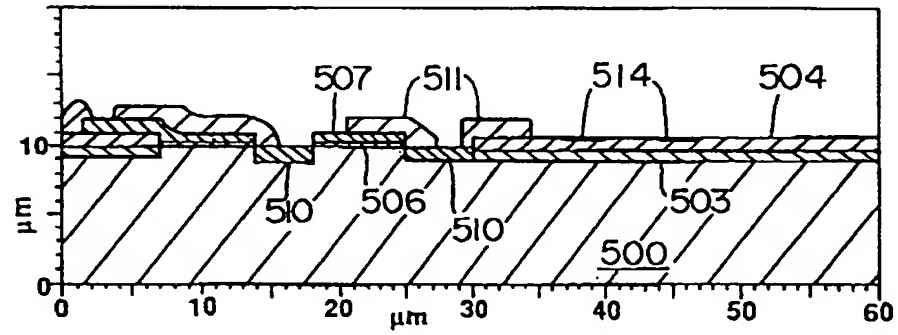


FIG.99

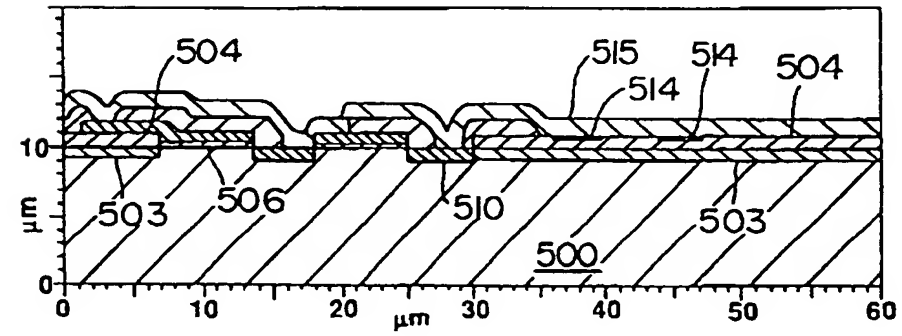


FIG.100

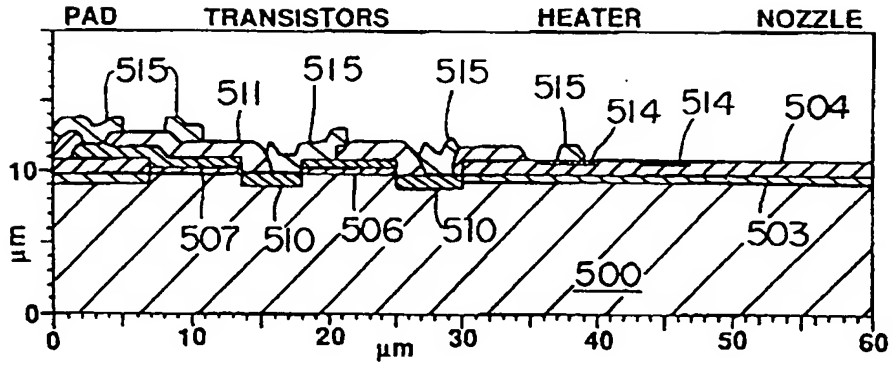


FIG.101

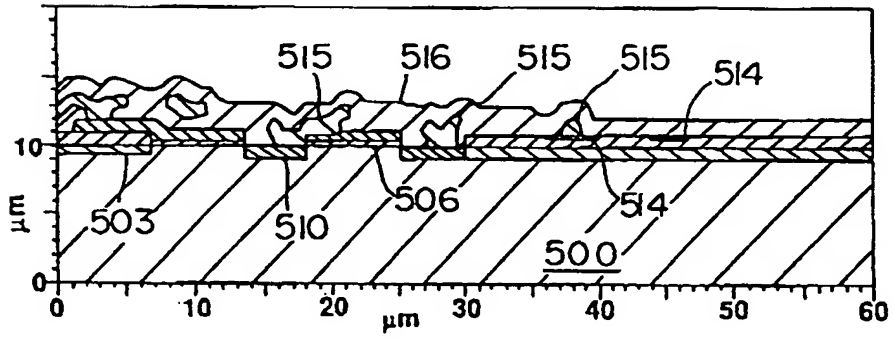


FIG.102

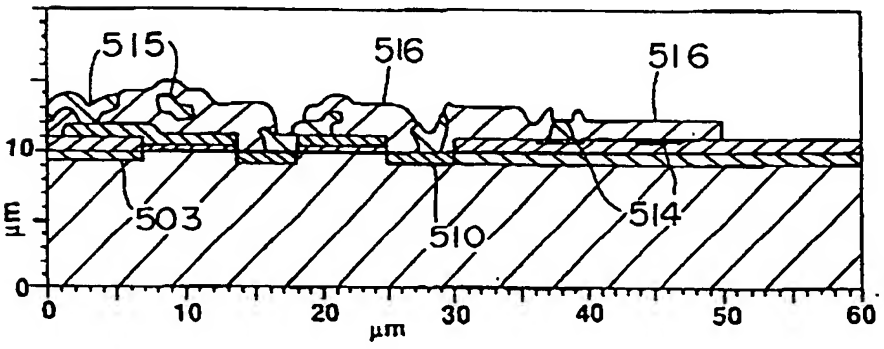


FIG.103

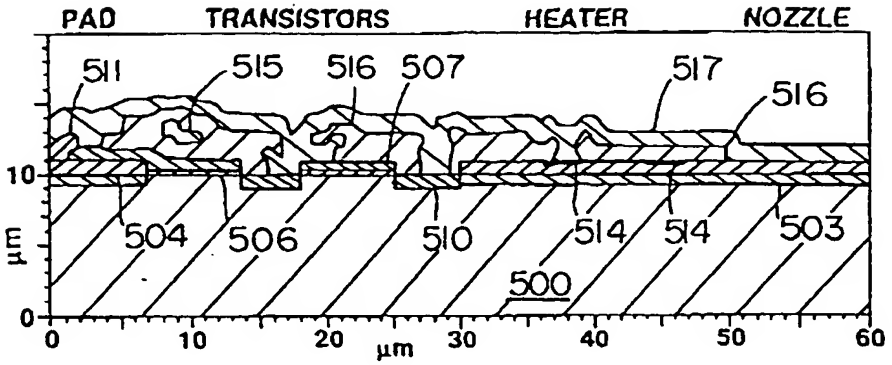


FIG.104

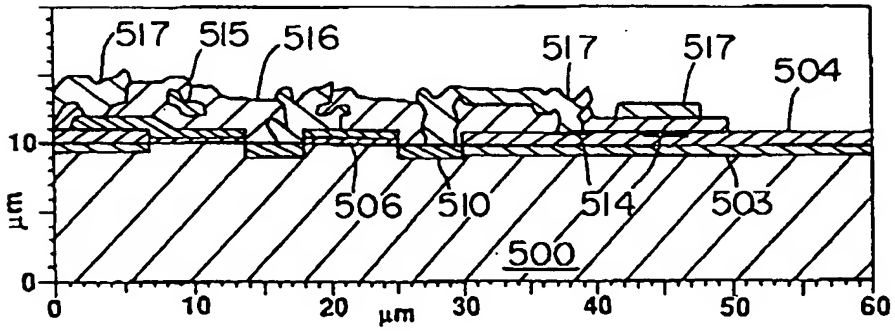


FIG.105

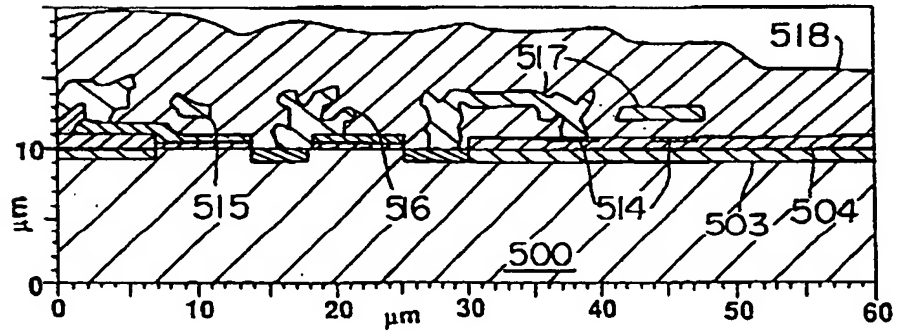


FIG.106

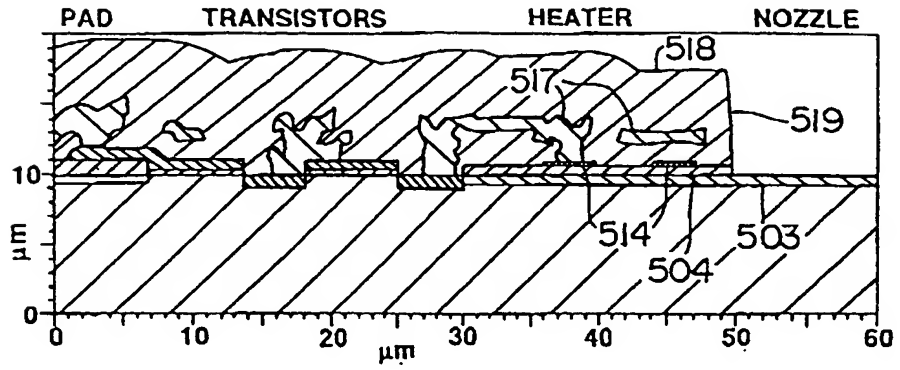


FIG.107

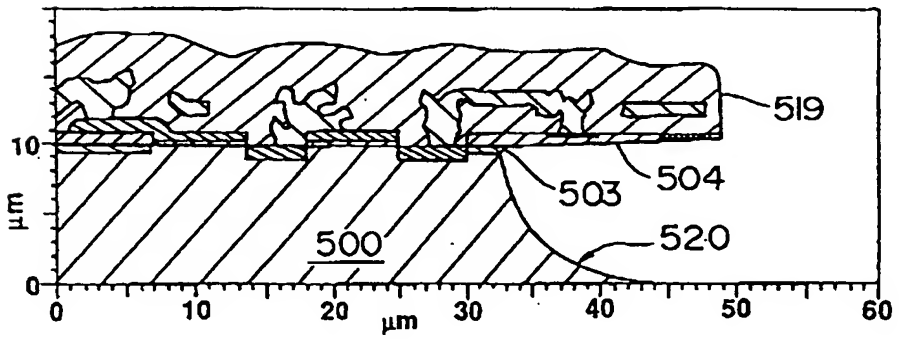


FIG.108

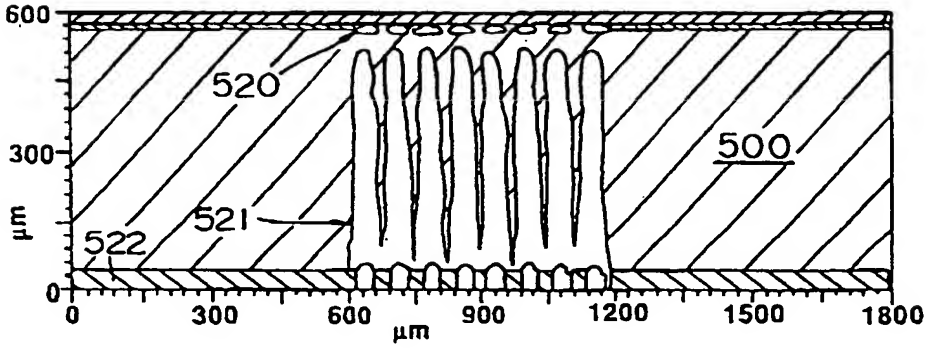


FIG.109

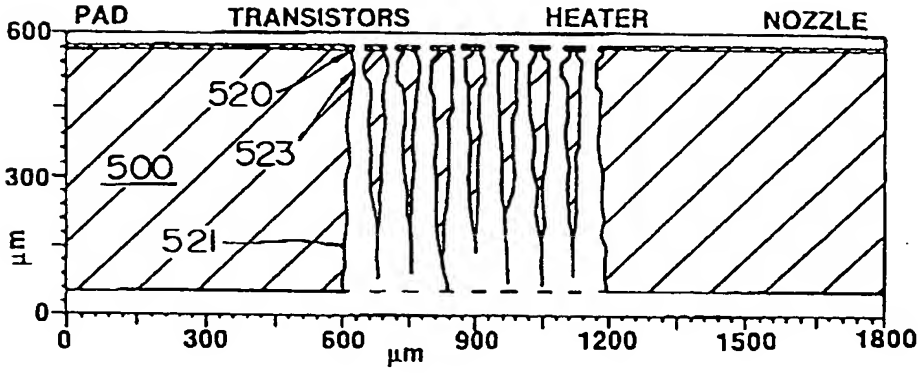


FIG.110

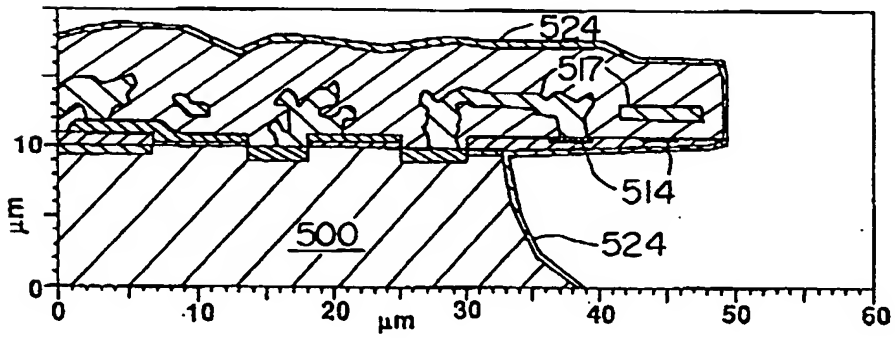


FIG.111

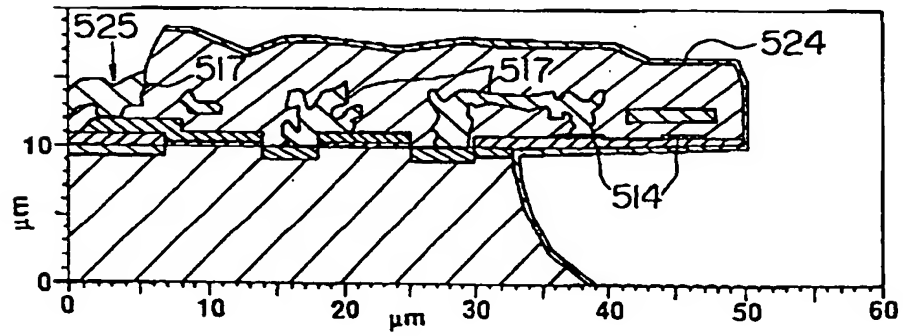


FIG.112

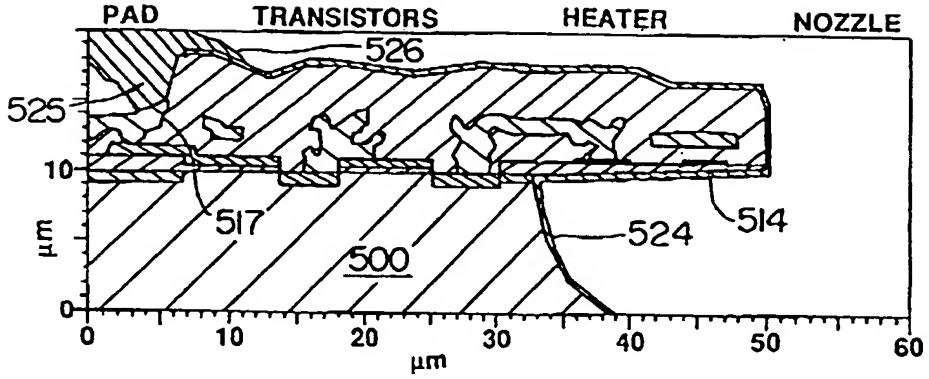


FIG.113

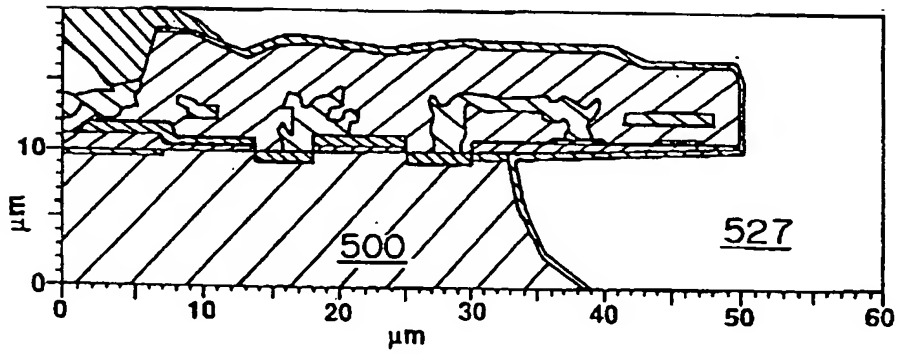


FIG.116

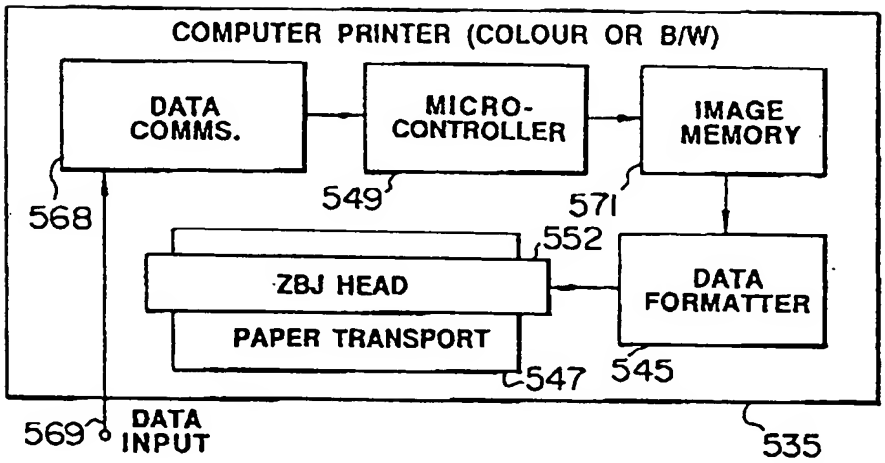


FIG.117

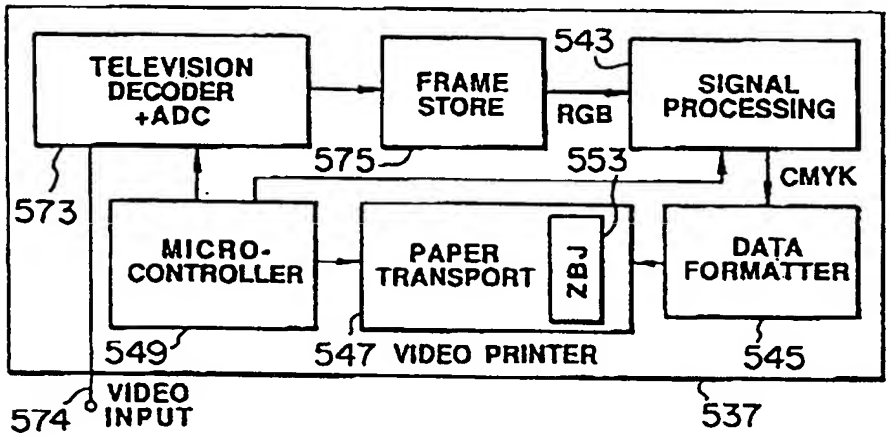


FIG.118

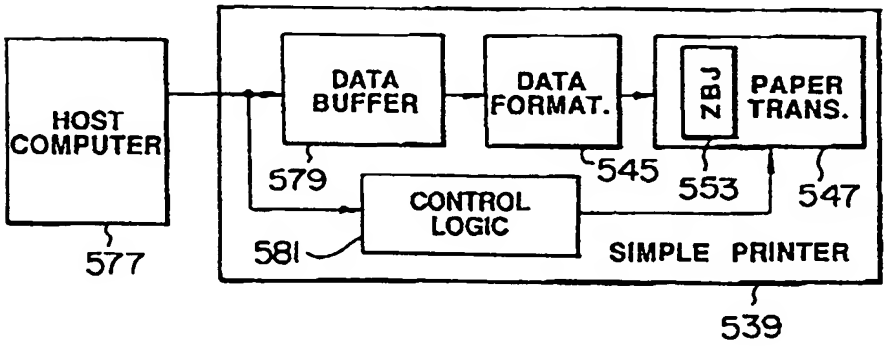


FIG. 114

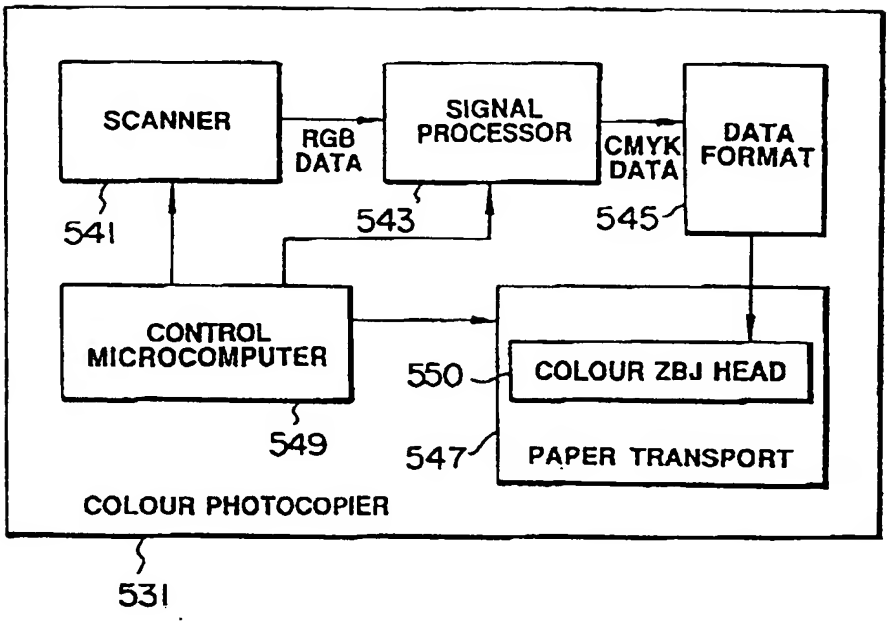
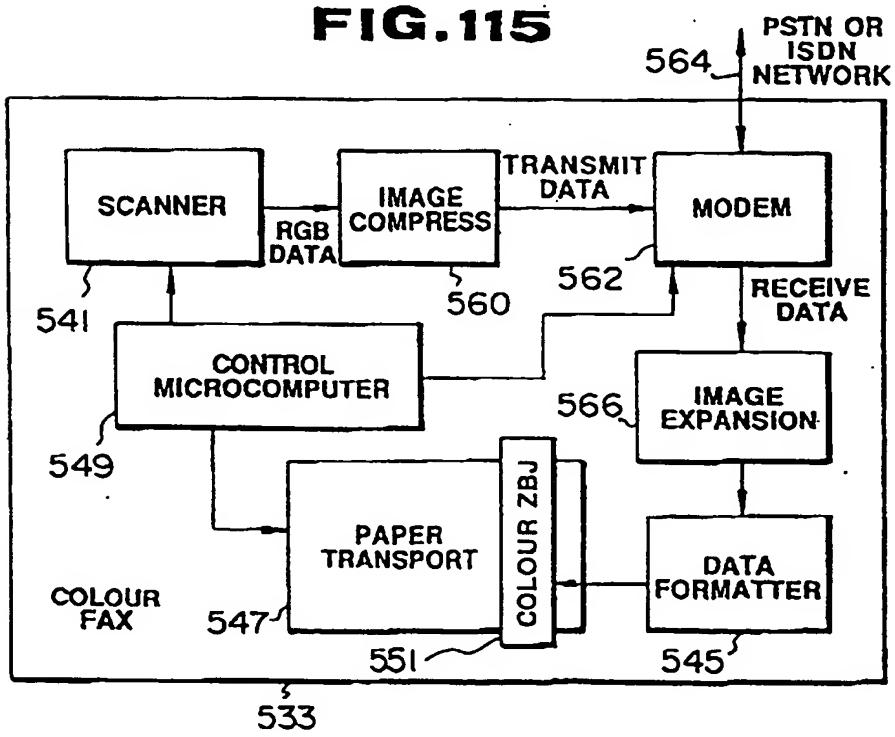


FIG. 115



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EUROPEAN SEARCH REPORT

Application Number

EP 92 10 1474

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	PATENT ABSTRACTS OF JAPAN vol. 12, no. 466 (M-772)7 December 1988 & JP-A-63 191 644 (SEIKO EPSON CORPORATION) 9 August 1988 * abstract *	1	B41J2/05
A	EP-A-0 244 214 (HEWLETT-PACKARD COMPANY) * page 5, line 25 - page 7, line 6; figures 3,4,9,10 * * page 9, line 19 - page 10, line 14 *	2,3,5,6	
A	EP-A-0 321 075 (HEWLETT-PACKARD COMPANY) * abstract; figures * * page 3, line 16 - page 4, line 31 *	2,3,5,6	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			B41J

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	06 MAY 1992	ROBERTS N.

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